Sapienza PhD in ICT

Doctoral program in Information and Communications Technologies at Sapienza Università di Roma, Rome, Italy

First Year Doctoral Program Form

LAST NAME	**Stazi**
NAME	**Giulia**
CURRICULUM	**Electronics Engineering**
DOCTORAL CYCLE	**XXXII**

The Doctoral Program Form contains, year by year, the description of the PhD program of each Doctoral student. This form must be submitted to the PhD coordinator with roughly the following timing:

- by the end of February of the first year for first year students
- before the admission to the second year by perspective second year students
- before the admission to the third year by perspective third year students

The Doctoral Program Proposal is approved by the PhD board shortly after submission. The Doctoral Program requirements place formalized emphasis on methodology and mastery of fundamental and applied engineering systems concepts. A Doctoral Program Proposal should be constructed in agreement with the Faculty mentor, that is the supervisor or tutor, by complying to the requirements, described in the Tables below.

ADVANCED COURSES: 12 CREDIT FORMATION UNITS (CFU)[1]
Only courses/schools providing a final verification test with pass/fail outcome certified by instructor can be included here.

Title	Type	Duration / period	CFU[2]	Motivation for selection
Programming of digital systems	Master Degree course	Duration: 1 Semester Occurence: Feb-May 2017	6	The course offers know how of embedded programming and and SW/HW interface implementation. This competencies are required for covering part of the PhD program.
PRINCE2® Foundation	Doctoral course	Duration: 3 days Occurence: 19-21 June 2017	6	Mandatory course.
Total CFU			12	

SEMINARS AND LABORATORY ACTIVITIES: 6 CFU[3]

Activity	Type	Duration / period	CFU[4]	Motivation for selection
Digital Design Verification training course	seminar	May 2017 2 days	1	The seminar offers useful know how of formal verification techniques possibly used in the PhD program
Digital HW/SW partitioning and programming	Laboratory	May 2017	1	The laboratory course offers know how on typical HW/SW interaction and function partitioning on embedded systems
Attendance to the conference "Applications in Electronics Pervading Industry, Environment and Society"	International Conference	Sept 2017, 3 days	2	The Conference intends to provide an opportunity of reciprocal meeting and knowledge on outstanding industrial and research activities for academicians, practitioners, and managers who operate in the field of electronic applications.

[1] Please insert lines as required/appropriate, and for each line complete each column of the Table.
[2] Indicate here the CFUs that can be accounted for as a result of the successful completion of the activity; for Master Degree courses, assume 1 CFU = 8 teaching hours + 12 homework/study hours, for a total of 20 hours. This rule can be slightly adjusted for other types of courses/activities (e.g., PhD courses may require slightly less hours per CFU)
[3] Please insert lines as required/appropriate, and for each line complete each column of the Table.
[4] Indicate here the CFUs that can be accounted for as a result of the successful completion of the activity; as a rule of thumb, assume 1 CFU = 20 working hours.

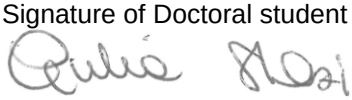
Attendance to the IEEE "PRIME" conference	International Conference	June 2017, 3 days	2	A comprehensive presentation of outstanding research work in electronics especially done by PhD students
Total CFU			6	

ADDITIONAL INDEPENDENT FORMATION AND RESEARCH ACTIVITIES: 6 CFU[5]
Indicate activities that extend and complement the mandatory activities listed above

Activity	Type	Duration / period	CFU[6]	Motivation for selection
Advanced simulation of digital platforms	Laboratory	Jan-Apr 2017	6	Acquiring competency on advanced simulation environments (instruction level emulation, dynamic code translation) for complex digital platforms is fundamental for the Phd research program.
Total CFU			6	

RESEARCH ACTIVITY: 36 CFU	
Research area	Energy-efficient design of digital VLSI systems.
Research topic	Study and the development of innovative strategies for approximate computing, an emerging technique in digital system design that aims at lowering energy consumption by allowing controlled computational faults in the application, reaching new trade-off between energy savings and accuracy.
Framework of the proposed research topic	Step 1: characterization and modeling of approximate computing technique. Fundamental to the activity is the study of the relationships between energy savings (that depends on circuit parameters) and the amount of allowed errors (that depends on the application and on the algorithm). This research phase involves simulations at circuit level (HSpice, Ngspice) and / or logic level in order to characterize the relationship between energy savings and the degree of approximation.
Research environment	Expected collaborations with ETH Zurich (prof. L.Benini) and Univ. of Singapore (prof. Alioto)

FACULTY MENTOR (TUTOR OR SUPERVISOR)	
Prof. Dr.	Francesco Menichelli
Supervisor signature for approval	

Signature of Doctoral student 

Date 11/04/2017

[5] Please insert lines as required/appropriate, and for each line complete each column of the Table.
[6] Indicate here the CFUs that can be accounted for as a result of the successful completion of the activity; as a rule of thumb, assume 1 CFU = 20 working hours.