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Analysis and design of low-power data converters

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Abstract

In a large number of applications the signal processing is done exploiting both analog and digital signal processing techniques, in the past digital and analog circuits were made on separate chip in order to limit the interference and other side effects, but the actual trend is to realize the whole elaboration chain on a single System on Chip (SoC). This choice is driven by different reasons such as the reduction of power consumption, less silicon area occupation on the chip and also reliability and repeatability. Commonly a large area in a SoC is occupied by digital circuits, then, usually a CMOS short-channel technological processes optimized to realize digital circuits is chosen to maximize the performance of the Digital Signal Proccessing (DSP). Opposite, the short-channel technology nodes do not represent the best choice for analog circuits. But in a large number of applications, the signals which are treated have analog nature (microphone, speaker, antenna, accelerometers, biopotential, etc.), then the input and output interfaces of the processing chip are analog/mixed-signal conversion circuits. Therefore in a single integrated circuit (IC) both digital and analog circuits can be found. This gives advantages in term of total size, cost and power consumption of the SoC. The specific characteristics of CMOS short-channel processes such as:

- Low breakdown voltage (BV) gives a power supply limit (about 1.2 V).
- High threshold voltage V_{TH} (compared with the available voltage supply) fixed in order to limit the leakage power consumption in digital applications (of the order of 0.35 / 0.4V), puts a limit on the voltage dynamic, and creates many problems with the stacked topologies.
- Threshold voltage dependent on the channel length $V_{TH} = f(L)$ (short channel effects).
- Low value of the output resistance of the MOS (r_0) and gm limited by speed saturation, both causes contribute to achieving a low intrinsic gain $g_m r_0 = 20$ to 26dB.
- Mismatch which brings offset effects on analog circuits.

make the design of high performance analog circuits very difficult. Realize low-power circuits is fundamental in different contexts, and for different reasons: lowering the power dissipation gives the capability to reduce the batteries size in mobile devices (laptops, smartphones, cameras, measuring instruments, etc.), increase the life of remote sensing devices, satellites, space probes, also allows the reduction of the size and weight of the heat sink. The reduction of power dissipation allows the realization of implantable biomedical devices that do not damage biological tissue. For this reason, the analysis and design of low power and high precision analog

circuits is important in order to obtain high performance in technological processes that are not optimized for such applications. Different ways can be taken to reducing the effect of the problems related to the technology:

- Circuital level: a circuit-level intervention is possible to solve a specific problem of the circuit (ie. Techniques for bandwidth expansion, increase the gain, power reduction, etc.).
- Digital calibration: it is the highest level to intervene, and generally going to correct the non-ideal structure through a digital processing, these techniques are based on models of specific errors of the structure.
- Definition of new paradigms.

This work has focused the attention on a very useful mixed-signal circuit: the pipeline ADC. The pipeline ADCs are widely used for their energy efficiency in high-precision applications where a resolution of about 10-16 bits and sampling rates above hundreds of Mega-samples per second (telecommunication, radar, etc.) are needed. An introduction on the theory of pipeline ADC, its state of the art and the principal non-idealities that affect the energy efficiency and the accuracy of this kind of data converters are reported in Chapter 1. Special considerstion is put on low-voltage low-power ADCs, in particular for ADCs implemented in deep submicron technology nodes side effects called short-cannel effects exist opposed to older technology nodes where undesired effects are not present. An overview of the short channel effects and their consequences on design, and also power consuption reduction techniques, with particular emphasis on the specific techniques adopted in pipelined ADC are reported in Chapter 2. Moreover, another way may be undertaken to increase the accuracy and the efficiency of an ADC, this way is the digital calibration. In Chapter 3 an overview on digital calibration techniques, and furthermore a new calibration technique based on Volterra kernels are reported. In some specific applications, such as software defined radios or micropower sensor, some circuits should be reconfigurable to be suitable for different radio standards or process signals with different charateristics. One of this building blocks is the ADC that should be able to reconfigure the resolution and conversion frequency. A reconfigurable voltage-scalable ADC pipeline capable to adapt its voltage supply starting from the required conversion frequency was developed, and the results are reported in Chapter 4. In Chapter 5, a pipeline ADC based on a novel paradigm for the feedback loop and its theory is described.

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Chapter 1

Introduction

1.1 Analog to Digital Converters

Technology scaling has enabled the capability to integrate the whole signal processing chain in the same chip, this allows the digital treatment of the signal that provides accurate processing and low power consumption, but the physical quantities from which the signals are derived have analogue nature, thus analog to digital converters (ADC) are required to interface the analog to the digital world. In a mixed-signal system the ADC could be the main cause of waste of energy. For this reason a reduction of the power consumption of an ADC is welcome, because it allows the possibility to implement mixed-signal systems in low-power environment. Over the years several ADC architectures have been developed to optimize specific features, such as resolution, conversion speed and power consumption. Each type of converter structure achieves optimal power consumption for a specific conversion frequency or resolution interval.

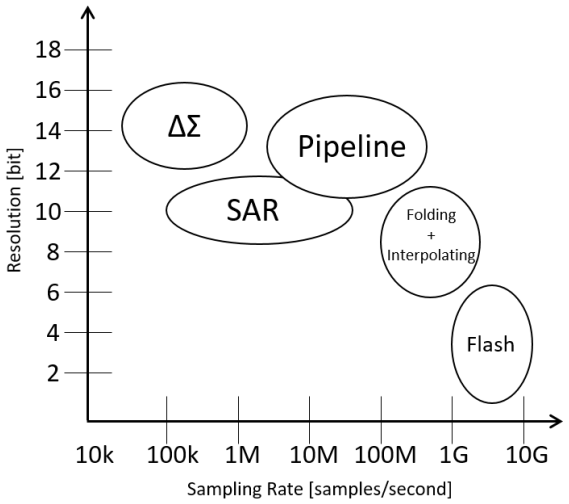

Figure 1.1. resolution sampling rate ADC structures

Figure 1.1 show the sampling frequency and resolution ranges where we can find each kind of ADC structure. We can clearly discern that Flash ADCs reach the fastest conversion frequencies, but with a limited resolution. Conversely the best resolution performance can be obtained only by $\Delta\Sigma$ ASCs but the conversion frequencies attained are very limited. There are different middle ground, such as Successive Approximation Register (SAR), Time-Interleaved and pipeline ADCs. Each Structure has been proposed to optimise a specific point, such as power consumption, resolution, conversion frequencies and area. In table 1.1 are reported the main charateristics for the different ADC structures.

Architecture	Latency	Speed	Accuracy	Area
Flash	Low	High	Low	High
SAR	Low	Low-medium	Medium-High	Low
Folding+interpolating	Low	Medium-High	Medium	High
Delta-Sigma	High	Low	High	Medium
Pipeline	High	Medium-High	Medium-High	Medium

Table 1.1. Resolution and sampling rate of different ADC structures

In Table 1.2 is reported a literature survey on different ADC structure published during the period that this work is being carried out. As shown in table the best speed performance are achieved not only by Flash ADCs, but also by time-interleaved system that uses several SAR or pipeline ADCs as subconverter. Furthermore aso high speed $\Delta\Sigma$ ADCs have been in the spotlight during the considered period.

The results published by ISSCC and VLSI in the last two decades are reported in figure 1.2 and 1.3. The figure spots the energy efficiency (defined in section 1.6) and the conversion frequency reached by the reported works. The figures bring out the energy efficirìency against the absolute speed. Since both the Walden and the Shreier FOM (the Walden and the Shreier Figure of merit are defined in 1.6) work well only across a limited range of SNDR, separate plot for FOM_S and FOM_W has been produced. For low-resolution designs, the FOM_W plot is more suitable, whereas the FOM_S plot does a better job at rewarding high resolution designs that also push bandwidth. The envelope lines included in the FOM vs. Speed plots are constructed as follows:

1. Identify the 5 data points with the best FOM (regardless of speed) and average them. This defines the "DC" value of the envelope.

2. Identify the 5 best data points with the best "combination2 of FOM and speed. For FOM_W, this means FOM_W/f_{snyq}. For FOM_S, this means $FOM_S + 10log(f_{snyq})$. The average of these defines the locations of the 10dB/decade rise/drop lines in the FOM plots.

Year	TYPE	Technology	Author	P[mW]	fs[MHz]	FOM_W [$\frac{fJ}{conv}$]
2014	Pipe, SAR	0,18	A. Bannon	30,5	5	-
2014	SAR	0,09	Y. Chen	0,0002	0.255	-
2014	Pipe	0,18	H. Venkatram	6	30	47,7
2014	Subranging	0,065	K. Yoshioka	6	820	89,8
2014	ΔΣ VCO	0,065	B. Young	38	1280	-
2014	ΔΣ	0,02	S. Ho	23	2810	-
2014	ΔΣ	0,18	A. Bandyopadhyay	21	57.5	-
2014	ΔΣ	0,09	C. Weng	4,3	300	-
2014	Pipe	0,18	H. Venkatram	6	30.0	47,7
2014	Pipe, SAR, TI	0,028	B. Verbruggen	2,3	200	4,4
2014	Pipe, SAR	0,065	C. Lin	5,3	210	20,7
2014	Pipe, SAR	0,04	Y. Zhou	4,96	160	17,5
2015	SAR	0,18	S. Jeong	0,00012	10	-
2015	SAR	0,014	C. C. Lee	4,3	70	26,7
2015	SAR	0,065	Z. Chen	0,121	50	-
2015	SAR, VCO	0,045	J. P. Mathew	3,4	200	8,1
2015	SAR, TI	0,028	Y. Duan	381	46000	452,9
2016	SAR	0,028	K. Obata	0,0371	0,1	-
2016	SAR, VCO	0,04	A. Sanyal	0,35	36	-
2016	SAR, TI	0,016	Yohan Frans	280	2800	150,9
2016	SAR, TI	0,065	Jae-Won Nam	37,7	1600	7,2
2016	Pipe, SAR, TI	0,028	Yuan-Ching Lien	0,0146	800	17,3
2016	Flash	0,028	Bharath Raghavan	0,095	10000	330,7
2016	SAR, TI	0,028	Benwei Xu	0,023	24000	20,9
2016	SAR. TI	0,016	Ying-Zu Lin	8,2	1600	11,2
2016	Pipe, TI	0,028	Ahmed M.A. Ali	2300	5000	398,5
2017	ΔΣ	0,028	I.H. Janget	4,2	320	-
2017	ΔΣ, VCO	0,04	S. Li	0,524	330	-
2017	ΔΣ	0,04	M. B. Dayanik	233	5000	237,2
2017	Pipe, SAR, TI	0,016	E. Martens	3,6	303	5,0
2017	Pipe	0,028	K.J. Moon	6	500	21,5
2017	Pipe	0,028	J. Lagos	14,2	600	36,0
2017	Pipe, SAR	0,04	Y. Lim	2,3	100	-
2017	SAR, Pipe	0,18	D. Hummerston	11,4	2	-
2017	Flash	0,065	S. Zhu	21	2000	240,5

Table 1.2. Literature survey on ADC in the years 2014 and 2017

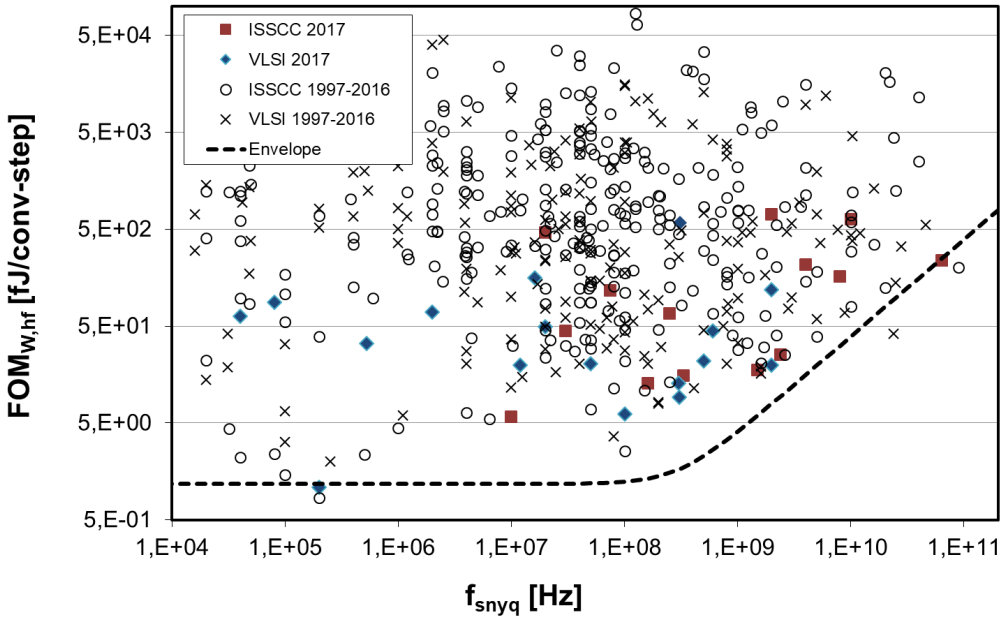

Figure 1.2. Figure Of Merit vs Speed in ADC

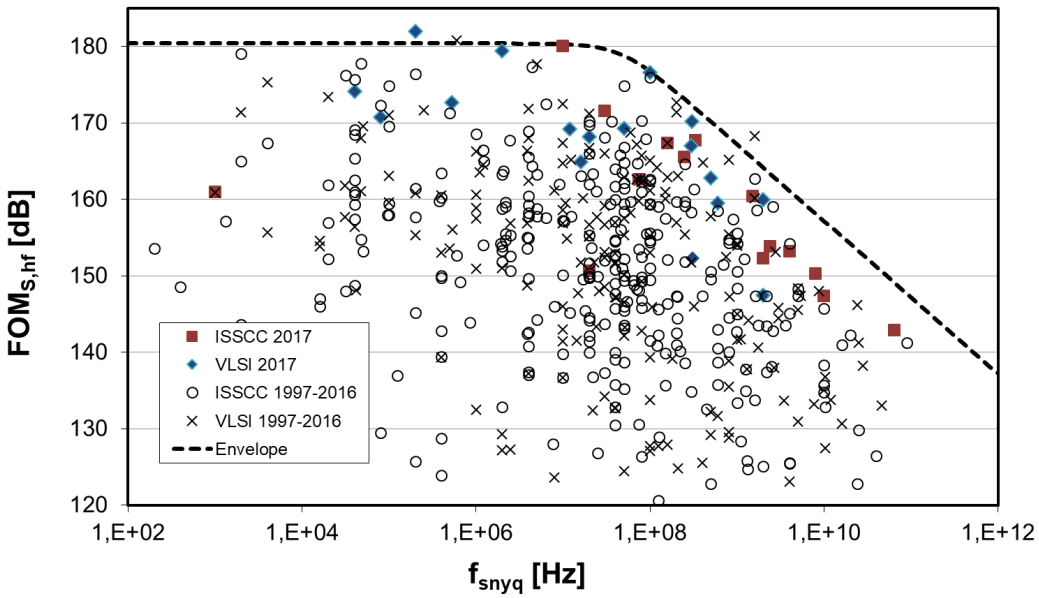

Figure 1.3. Shreier FOM vs frequency

Between the different structures one of the most interesting is the pipeline ADC because it can reach conversion frequencies and resolutions that make this structure suitable for telecom, radar and biomedical applications. This Chapter continues with an overview of the principal architectures of ADC converter and for each type is kept the focus on the pros and cons respect to the pipeline converter.

1.1.1 Flash ADC

Many different ADC architectures have been developed over the years, each with different tradeoffs respects to power consumption, speed, and resolution. Most of this structures are derived from the Flash ADC, or make use of Flash ADC in their implementation.

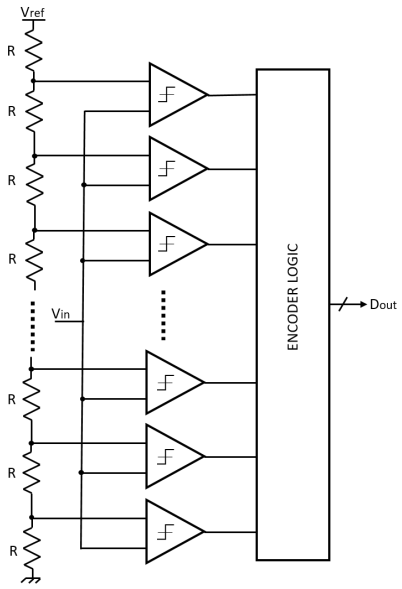

Figure 1.4. Flash ADC structure

Figure1.4 shows the principle scheme of a Flash converter. Flash ADC converts an analog signal into a digital one by comparing the signal with fixed reference values, determining in which interval of the 2^N is the input signal. Mapping the thermometer code to its binary equivalent forms a N binary representation of the input signal [1]. A flash ADC has a large bank of comparators, each consisting of wideband, low-gain preamps followed by a latch. The preamps must provide gains that do not need to be linear or accurate; only the comparator's trip points must be accurate. As a result the speed of a flash ADC can not be reached by any other ADC structure. Another key advantage in Flash ADC architecture is the latency of only one clock cycle, an furthermore does not matter for the linearity of the comparators involved in the structure. The main drawback of Flash converter is due to the number of the comparators required, in fact, the number of comparators doubles for every resolution bit added; at the same time, each comparator must be twice accurate, thus large devices are required to suppress process variation effects, thus high resolution Flash ADCs require too high silicon area, and also the power consumprion makes the flash ADC unsuitable for some applications where the energy efficiency plays a fundamental role for the feasibility.

1.1.2 ADC Pipeline

Some of the limitations of the flash ADC are overcome by the pipeline ADC.

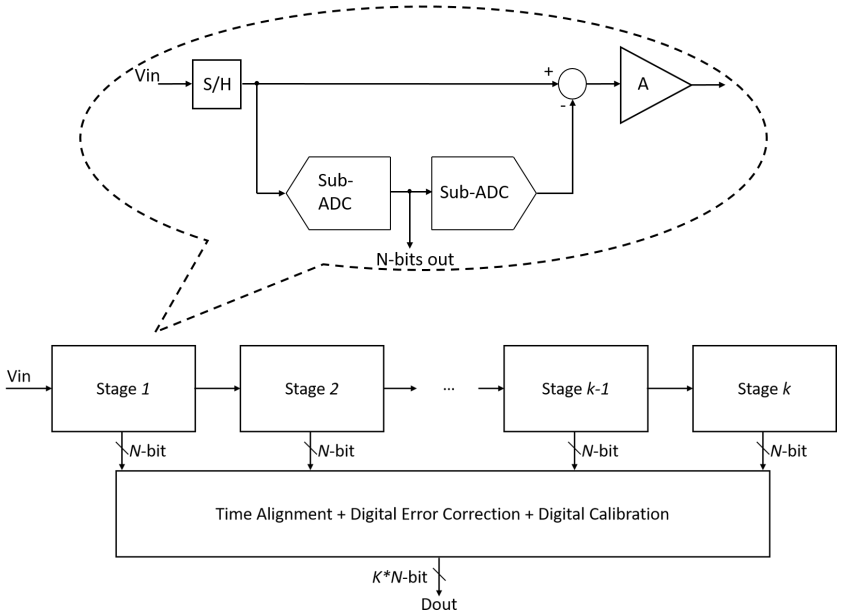

Figure 1.5. Pipeline ADC structure

A pipeline ADC is composed by a chain of N_s stages, and the conversion of a sample is splitted in N_s steps. Each stage of the pipeline takes as input an analog signal and provides as output a digital signal that represents a partial conversion of the signal, and also provides an analog output that will be refined by the successive stage. These stages are composed by a sub-ADC, a sub-DAC and an error amplifier. In figure 1.5 a principle schematic is shown. In each stage the analog input, V_{in}, is first sampled and held steady by a sample-and-hold structure, while the flash sub-ADC in the first stage quantizes it in N bits (N bit is the number of conversion bit of each stage). The output of the sub-ADC is taken as input by the sub-DAC, and the analog output is subtracted from the input. This "residue" is the quantization error of the sub-ADC and then this signal is multiplied by a factor 2^N and fed to the next stage. This gained-up residue continues through the pipeline, providing N bits per stage until it reaches the last sub-ADC, which resolves the last N bits. Because the bits from each stage are determined at different points in time, all the bits corresponding to the same sample are time-aligned with shift registers before being fed to the digital-error-correction logic. Note that when a stage finishes processing a sample, determining the bits, and passing the residue to the next stage, it can then start processing the next sample received from the sample-and-hold embedded within each stage. This pipelining action is the reason for the high throughput, but conversely to the flash, the pipeline ADC is affected by data latency, because

each sample must propagate through the entire pipeline before all its associated bits are available for combining in the digital-error-correction logic. Moreover, the accuracy and the linearity required on the comparator of the pipeline ADC place some constraints that figure out pipelined ADC cannot match the speed of a well-designed flash ADC.

1.1.3 SAR ADC

An arising interest in the last years is posed on successive approximation register (SAR) ADCs, that reduce dramatically the power consumption respect to the flash ADC. In a SAR-ADC, the bits are decided by a single high-speed, high-accuracy comparator bit by bit, from the most significative bit (MSB) down to the least significative bit (LSB).

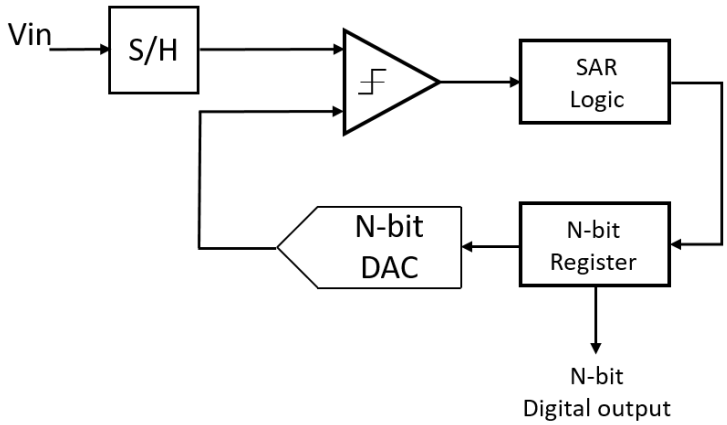

Figure 1.6. SAR ADC block diagram

Figure 1.6 show a SAR ADC structure. A Sample-and-Hold holds the analog input while the sequential binary search is carried out. The SAR ADC compares the analog input with a digital to analog converter (DAC), whose output is updated by previously decided bits and successively approximates the analog input. At the beginning of the conversion phase, the register is initialized to midscale, which forces the decision threshold of the comparator to be $V_{ref}/2$. Based on the result of the comparator the MSB remains '1' if the analog value is above $V_{ref}/2$, or is changed to '0' if the input is below $V_{ref}/2$. By successively repeating the next bit is initialized to '1', and the decision threshold will be $V_{ref}/4$ or $3V_{ref}/4$. The iterative algorithm is repeated N times, where N is the resolution of the SAR ADC. The successive approximation algorithm makes the SAR ADC more energy efficient respect to the Flash ADC which use a brute force approach to perform the conversion. The other significant advantage of the SAR ADC is that it uses only one comparator, and a few other analog components for a N-bit conversion. The serial nature of SAR limits its operating speed, and still slower for very high resolutions (14 to 16 bits).

This issue is solved in pipelined ADC that employs a parallel structure in which each stage works on 1 to a few bits (of successive samples) concurrently. Although there is only one comparator in a SAR, this comparator must be fast, clocked at approximately the product of number of bits for the sample rate $f_{CK} = Nf_S$, and as accurate as the ADC itself. This is another issue overcomed in pipeline structure where none of the comparators inside a pipelined ADC needs this degree of speed or accuracy. Thus although the SAR ADC allows for a significant reduction of the analog components it comes at the cost of restricting the maximum sampling rate to only a fraction of the maximum available in a given technology. It should be noted that while the SAR determines 1-bit of the final digital output every clock cycle, the DAC is required to settle to the full accuracy of the ADC every clock cycle. Also, the comparator is required to be able to resolve inputs as small as the LSB of the ADC. As a result, much effort is required to optimize the DAC and the comparator blocks for high speed and high accuracy.

1.1.4 Sigma-Delta ADC

The Sigma Delta ($\Sigma\Delta$) converter is a completely different kind of converter. First of all, it is an over-sampling converter: the signal occupies only a fraction of the Nyquist band. Second, it uses a special feedback loop to concentrate the power of the nonlinear terms in bands outside that of the input signal. Finally, it uses digital filters and decimators to filter the non-linear terms and reduce the conversion speed to the Nyquist limit. Figure 1.7 shows the basic architecture of a $\Delta\Sigma$ ADC. This architecture is called "first-order single-bit" converter, because it uses only one feedback loop, and this loop uses a single-bit DAC.

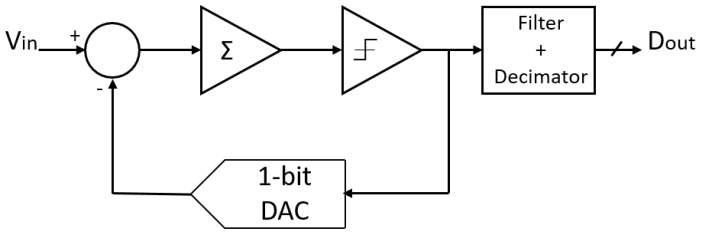

Figure 1.7. $\Sigma\Delta$ ADC block diagram

The integrator is put into a feedback loop and, due to its high gain at low frequencies, it reduces the error at these frequencies (being the error the difference between the input analog voltage and the output digital voltage, converted by the DAC), and pushes all the errors at high frequencies. Despite the fact that the output voltage is a digital single-bit stream, and it doesn't seem to resemble the input continuous-time signal in the time domain, in the frequency domain the difference between input and output is concentrated at high frequencies. But if the

signal is at low frequencies, most of the distortion can be filtered, thus obtaining a high resolution converter. Traditionally, oversampling/sigma-delta-type converters commonly used in digital audio have a limited bandwidth of about 22kHz. Recently some high-bandwidth sigma-delta converters reached a bandwidth in the order of GHz with more than 16 bits of resolution.Sigma-delta converters trade speed for resolution. The need to sample many times (for example, at least 16 times, but often much higher) to produce one final sample causes the internal analog components in the sigma-delta modulator to operate much faster than the final data rate. The digital decimation filter is also nontrivial to design, and consumes a lot of silicon area.

1.2 Performance Characterization in ADC Converters

The goodness of an analog to digital converter may be characterised through different parameters, that can be grouped around three main lines which is static, dynamic and frequency domain performances. The static performance defines the goodness of the dc transfer function of the converter, that can be expressed theough two significant figure of merit as Differential Non Linearity (DNL) or Integral Non Linearity (INL). Dynamic performanes are related to the behaviour of the converter when a time variable input signal is applied as stimulus. Finally frequency domain performance defines the linearity of the converter or the effect of the noise in the frequency domine, the main figure of merit in this domain are the Total Harmonic Distortion (THD), the Signal to Noise Ratio (SNR) and their derived the Signal to Noise and Distortion Ratio (SNDR) and the Effective Number of Bits (ENOB). The different characteristics can be more or less interesting, based on the applications: for measure instruments are more important the static performances as the INL and DNL; in telecom field the frequency domain characteristics are more interesting because distortion has more impact on the signal than the static error quantifiable with INL and DNL. The Fast Fourier Trasform (FFT) on the output signal of an ADC (reconverted in analog domain by an ideal DAC) shows the distortion above a noise floor, thus the ratio $\frac{P_{signal}}{P_{distortion}}$ gives a measure of the linearity of the response of an ADC, the principal parameter that gives a measure of the distortion is the Total-Harmonic-Distortion (THD), that represents the ratio between the power of the singnal and the sum of all the spectral components distortion. Ideally an ADC does not introduce any distortion, thus the recostructed signal is affected only by quantization error. Also the noise as the distortion is a fundamental parameter, because defines the lower limit of the dynamic of the signal. The main parameter related to the noise is the Signal-to-Noise Ratio (SNR). By aggregating the effect of the noise and the distortion expressed by SNR and THD we obtain the Signal-to-Noise-and-Distortion-Ratio (SNDR), from the latter one is possible evaluare the

Effective-Number-of-Bits (ENOB) which is the number of information bits above the floor due to noise and distortion.

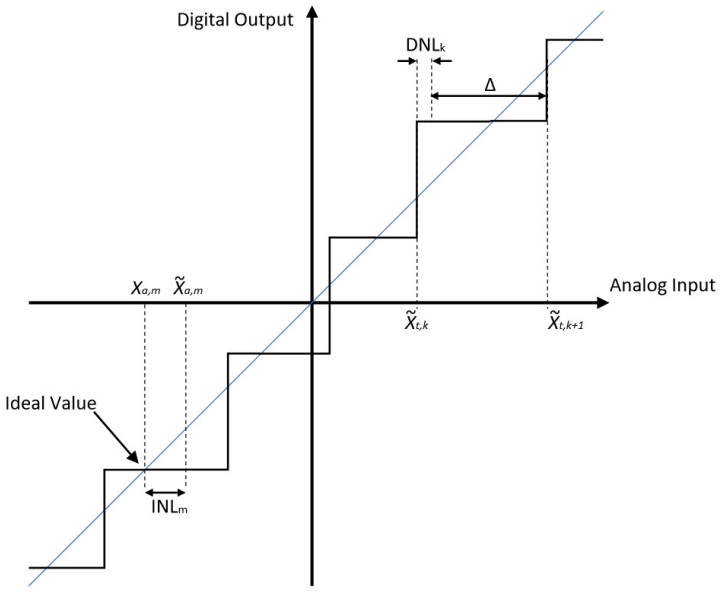

Figure 1.8. Transfer function of a non ideal ADC

To distinguish between the actual and ideal values in the data converters, all actual values are indicated with a ˜. This means that $X_{a,k}$ corresponds to the ideal analog value for digital code $X_{d,k}$ while $\tilde{X}_{a,k}$ corresponds to the actual value.

1.2.1 Static Characteristics

Static errors, that is those errors that affect the accuracy of the converter when it is converting static (dc) signals, can be completely described by just four terms. These are offset error, gain error, integral nonlinearity and differential nonlinearity.Each can be expressed in LSB units or sometimes as a percentage of the Full-Scale Range (FSR). The linearity of the ADC and its Sample-and-Hold may be limited for a several number of causes, such as nonlinear switch on resistance, clock feedthrough errors, finite amplifier gain, parasitic capacitors or any other error sources present in the circuit.

1.2.1.1 DNL

In an ideal ADC the input dynamic is divided in uniform steps Δ. In actual implementation the deviation of the step from the ideal value is called differential nonlinearity (DNL) error. The DNL is defined as the difference of two adjacent levels minus the ideal step size.

$$DNL_k = \widetilde{X}_{t,k+1} - \widetilde{X}_{t,k} - \Delta \tag{1.1}$$

Usually the DNL is normalized respect the ideal value of the step size Δ.

$$DNL_k = \frac{\widetilde{X}_{t,k+1} - \widetilde{X}_{t,k} - \Delta}{\Delta} \tag{1.2}$$

If the DNL exceeds 1 LSB, there is a possibility that the converter can become nonmonotonic. This means that the magnitude of the output gets smaller for an increase in the magnitude of the input. In an ADC there is also a possibility that there can be missing codes i.e., one or more of the possible 2^n binary codes are never output.

1.2.1.2 INL

The integral nonlinearity error shown in Figure 1.8 (sometimes seen as simply linearity error) is the deviation of the values on the actual transfer function from a straight line. This straight line can be either a best straight line which is drawn so as to minimize these deviations or it can be a line drawn between the end points of the transfer function once the gain and offset errors have been nullified. The second method is called end-point linearity and is the usual definition adopted since it can be verified more directly.

$$INL_k = \frac{\widetilde{X}_{a,k} - X_{a,k}}{\Delta} \tag{1.3}$$

The relation between INL and DNL is given by

$$INL_k = \sum_{l=1}^{k} DNL_l \tag{1.4}$$

1.2.1.3 Offset Error

The offset error is defined as the difference between the nominal and actual offset points. For an ADC, the offset point is the midstep value when the digital output is zero. This error affects all codes by the same amount and can usually be compensated for by a trimming process. If trimming is not possible, this error is referred to as the zero-scale error. The offset X_{offset} of a converter is given by

$$X_{offset} = \frac{1}{2^N} \cdot \sum_{K=0}^{2^N-1} (\widetilde{X}_{a,k} - Xa, k) \tag{1.5}$$

and represent the average of all the errors in the converter. To eliminate the offset from the INL calculations, the offset should be subtracted from all the analog values $\widetilde{X}_{a,k}$.

1.2.1.4 Gain Error

This error represents a difference in the slope of the actual and ideal transfer functions as shown in figure 1.9. This error can be linear or non linear. This error can also usually be adjusted to zero by trimming.

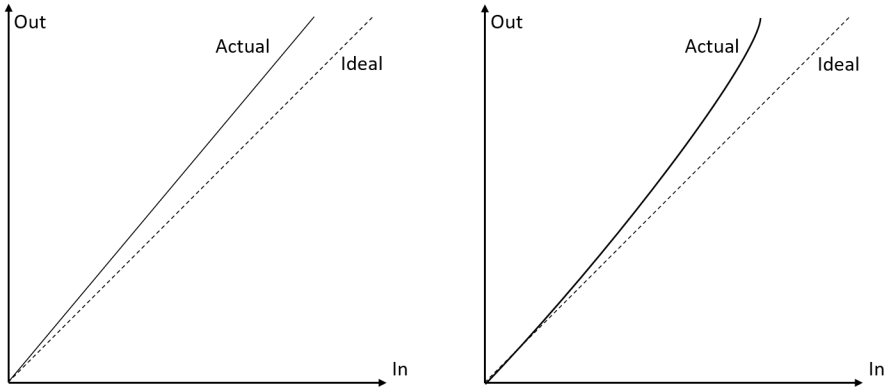

Figure 1.9. Linear and non linear gain error

The actual implementation can present two kind of differences compared to the ideal straight line: the actual output has a linear gain error as shown on the left in figure 1.9 and also non-linearity as in the right of the same figure. The linear gain error does not introduce distortion on the output signal, and can be written as:

$$\widetilde{X}_a = A \cdot X_a + X_{offset} \tag{1.6}$$

where A is the gain. The non-linear gain error is also given by

$$\widetilde{X}_a = A_1 \cdot X_a + A_2 \cdot X_a^2 + A_3 \cdot X_a^3 + \ldots + X_{offset} \tag{1.7}$$

the 1.3 can be rewritten taking in account the effect of gain error

$$INL_k = \frac{\widetilde{X}_{a,k} - (A \cdot X_{a,k} + X_{offset})}{A \cdot \Delta} \tag{1.8}$$

1.2.2 Frequency Domain Measures

To characterize a data converter, static performances are not sufficient, also is more convenient characterize the performance in the frequency domain as signal-to-noise ratio (SNR) and spurious-free dynamic range (SNDR).

1.2.2.1 Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio, due to the quantization error is defined as

$$SNR = \frac{P_s}{P_n} = \frac{(\Delta \cdot 2^{N-1})^2)/2}{\Delta^2/12} = 1.5 \cdot 2^{2N} \tag{1.9}$$

where P_s represent the average power of maximum input signal that not cause saturation; P_n is the average power of quantization noise. 1.9 can be rewritten in decibel

$$SNR_{dB} = 10 \cdot log\left(\frac{P_s}{P_n}\right) = 6.02 \cdot N + 1.76dB \tag{1.10}$$

SNR_{dB} is increased by 6 dB for each additional bit of conversion. For a single tone measurement the SNR is the ratio of the power of the input signal and the total noise power, excluding the harmonic components. In the ideal case the SNR value is determined only by the power of quantization error and signal, in real case additional noise source affect the system as example the termal noise and must be taken into account.

1.2.2.2 Spurious Free Dynamic Range (SFDR)

The same non idealities that generate INL and DNL in the static characterization, in case of sinusoidal input generate distortion. Different figures of merit can be defined to characterize the distortion. The ratio of the power of the signal and the power of the largest spurious is called spurious free dynamic range (SFDR), and is expressed as:

$$SFDR(dB_c) = 10 \cdot log\left(\frac{Signal\,Power}{Largest\,Spurious\,Power}\right) = 10 \cdot log\left(\frac{X_1^2}{X_s^2}\right) \tag{1.11}$$

where X_1 is the rms value of the fundamental and X_s the rms value of the largest spurious. In some cases the SFDR is defined with full scale input signal as:

$$SFDR(dB_{FS}) = 10 \cdot log\left[\frac{\left(\frac{FS}{2\sqrt{2}}\right)^2}{X_s^2}\right] \tag{1.12}$$

1.2.2.3 Harmonic Distorsion HD_K

The harmonic distortion referred to the k-th harmonic HD_k is the ratio between the power of the k-th harmonic and the power of the fundamental frequency of the signal

$$HD_K = 10 \cdot log\left(\frac{k_{-th}\,Harmonic\,Power}{Signal\,Power}\right) = 10 \cdot log\left(\frac{{X_k}^2}{{X_1}^2}\right) \tag{1.13}$$

where X_1 is the RMS power of the fundamental frequency and X_k is the RMS power value referred to the k-th harmonic.

1.2.2.4 Total Harmonic Distorsion

The Total Harmonic Distorsion (THD) is the ratio between the sum of th power of all the harmonics and the power of the fundamental frequency in the considered band.

1.2.2.5 Signal-to-noise and Distorsion Ratio (SNDR)

Summing up all the undesired terms such as quantization error (negligible), thermal noise and distortion, a quantity that describes the ratio between the power of the signal and the power of all the undesired terms can be defined. The signal-to-noise and distortion ratio (SNDR) is the ratio of the power of the fundamental and the total noise and distortion power

$$SNDR = 10 \cdot log\left(\frac{Signal\,Power}{Noise\,and\,Distorsion\,Power}\right) \tag{1.14}$$

1.2.2.6 Effective Number Of Bits (ENOB)

Based on SNDR measure is determined the effective number of bits (ENOB) of an ADC with a full scale sinusoidal input signal as

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{1.15}$$

both ENOB and SNDR measures are frequency and amplitude dependent. For small amplitude levels the performance are limited by the quantization noise, while for high input amplitude the distortion will limit the performance.

1.2.2.7 Dynamic Range

The Dynamic Range (DR) is defined as the interval between the minimum detectable signal and the full scale (FS) values.

$$DR = 10 \cdot \left(\frac{Maximum\,signal\,power}{Minimum\,signal\,power}\right) \tag{1.16}$$

The Dynamic range is limited upperly by the distortion that appears when the magnitude of the signal cover a significant portion of the signal dynamic of the converter, and is lower limited by the power of the noise that can cover the signal when this is too small.

1.2.2.8 Effective Resolution Bandwidth

An important parameter for the data converter is the signal bandwidth that can be handled. The bandwidth is limited by the analog bandwidth of the input circuits in the ADC thus the Sample-and-Hold, or by the Effective-Resolution-Bandwidth

(ERB) thus the ADC. The input signal frequency must be smaller than the Nyquist frequency (half the sampling frequency) to avoid aliasing in conventional applications of ADCs. The bandwidth can be larger than the Nyquist frequency for sub-sampling ADCs. To specify the frequency behaviour of the converter it is common to plot the SNDR, SFDR or SNR as function of input frequency as illustrated in 1.10. The effective resolution bandwith is the input frequency where SNDR has dropped 3dB (1/2 bit ENOB).

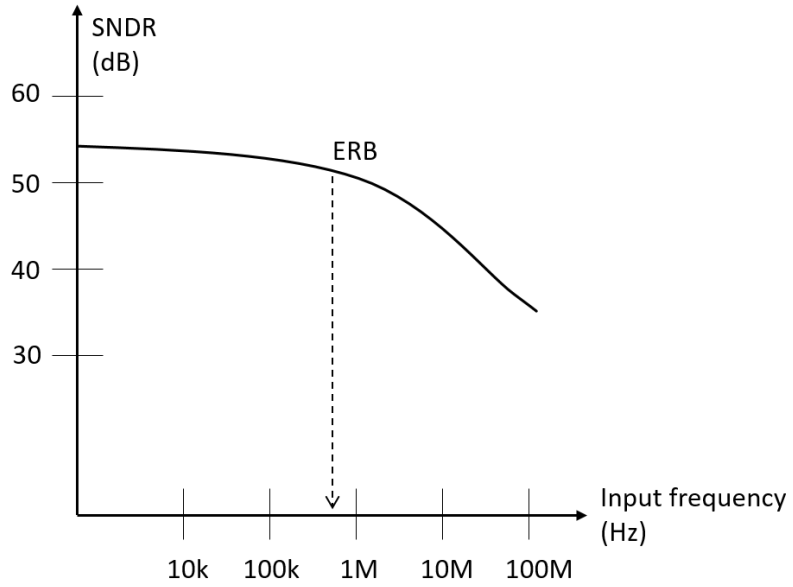

Figure 1.10. Effective Resolution Bandwidth

1.2.2.9 Inter-Modulation Distortion

When the input signal is multi-tone inter-modulation distortion (IMD) appears. Assume that the frequencies of the the input tone are respectively f_1 and f_2, and the sampling rate f_s, intermodulation disortion appear at frequency

$$(k \cdot f_1 + m \cdot f_2) mod (f_s/2) \tag{1.17}$$

where k and m are integer numbers, and further $k \neq 0$ and $f_1 \neq f_2$. The intermodulation distortion is calculated as

$$IMD = 10 \cdot log \left(\frac{\sum X_{k,m}^2}{X_0^2} \right) \tag{1.18}$$

where X_0 is the rms value of the fundamental, and $X_{k,m}$ is the rms value of the tones.

1.2.3 Dynamic Performance

Several unwanted effects appear when the input signal changes rapidly, these dynamic errors often are frequency dependent and increase when signal amplitude or frequency are increased. Moreover, the same static error that generates INL and DNL causes distortion when the input signal is time variable as example a sinusoidal input. Thus in some applications such as telecommunications this kind of information has much weight than the static errors.

1.2.3.1 Sampling Time Uncertainly

The dynamic performance of an ADC is limited by the precision of the sampling instant in the Sample-and-Hold circuit. Many unwanted phenomena such as switch imperfections, clock jitter, and signal-dependent delay can generate uncertainty on the sample instant.

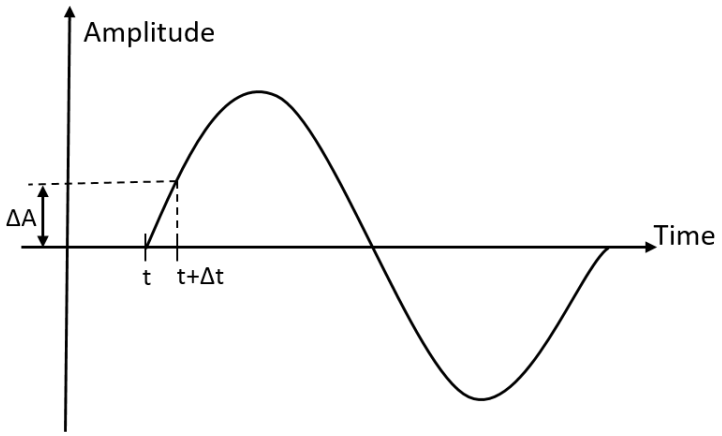

Figure 1.11. Sampling time uncertainty generates an error on the sampled signal

In figure 1.11 the desired sampling time is t but due to the circuit non-ideality the actual sampling time is $t + \Delta t$. This delay causes an error ΔA that depends on the slope of the input signal. For a sinusoidal input signal, the worst case is when zero crossing happens.

$$\Delta A_{max} = \Delta t \cdot \frac{\partial}{\partial t} V_{in}(t)|_{t=0} = \omega \cdot A \cdot cos(\omega t) \cdot \Delta t = \omega \cdot A \cdot \Delta t \tag{1.19}$$

where A is the amplitude of the sinusoid. The error increases linearly with frequency and is independent of the sampling frequency. Many techniques can be applied to reduce this error, for instance, the bottom plate sampling. Anyway, the performance is limited by clock jitter. Assuming the clock jitter as random noise with variance σ_t^2 the error power can be approximated as

$$v_{jn}^2 = \sigma_t^2 \cdot \frac{1}{T} \int_0^T \left(\frac{\partial}{\partial t} V_{in}(t) \right)^2 dt \tag{1.20}$$

where T is the integration time. For a sinusoidal input the power error is

$$v_{jn}^2 = (2\pi f_{in} A)^2 \sigma_t^2 / 2 \tag{1.21}$$

where A is the amplitude and f_{in} the frequency of the sinusoid. Thus the SNDR is limited by

$$SNDR_{lim} = 10 \cdot log \frac{1}{(2\pi f_{in} \sigma_t)^2} \tag{1.22}$$

and then also the ENOB is limited

$$ENOB_{lim} = \frac{10 \cdot log \frac{1}{(2\pi f_{in} \sigma_t)^2} - 1.76}{6.02} \tag{1.23}$$

SNDR is independent from the sampling frequency. The obtainable ENOB as function of the clock jitter σ_t is plotted for different input frequencies in figure 1.12. The figure shows the performance decreases rapidly for high sampling rate.

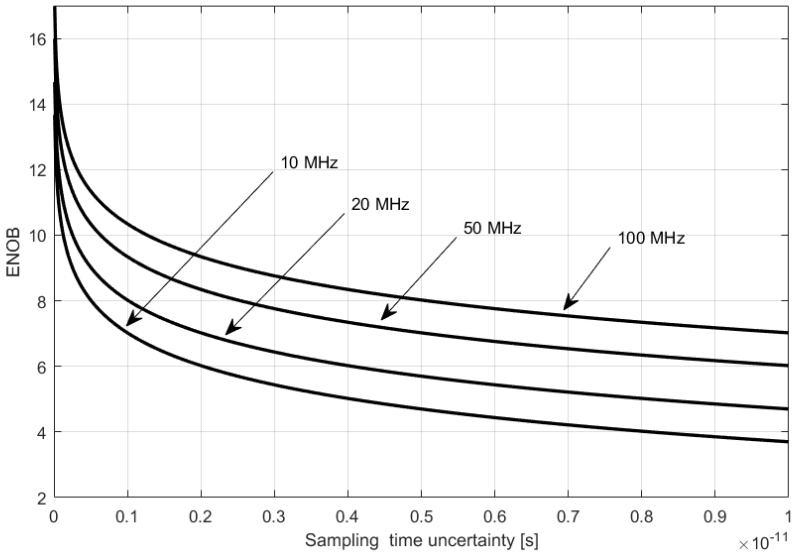

Figure 1.12. ENOB vs sampling time uncertainty for different value of sampling frequencies

1.2.3.2 Thermal Noise

A limiting factor in Sample-and-Hold circuit is the thermal noise. Commonly, in wideband circuits, the thermal noise is dominant on flicker noise because is folded back into the signal band by the sampling technique, this introduces a fundamental limitation. In Sample-and-Hold the thermal noise power is kT/C. Assuming as input a sinusoidal signal with amplitude V_{in}, the SNDR is

$$SNDR = 10 \cdot log\left(\frac{V_{in}^2}{2 \cdot kT} \cdot C\right) \tag{1.24}$$

The voltage swing is limited by the power supply voltage, then increasing the sampling capacitor is the only way to increase the SNDR. For moderate resolution the minimum capacitor size for the noise requirement is very small, and a larger capacitor value may be chosen for other reasons (such as process error that can generate mismatch that is area dependent). For high resolution a huge capacitor is required to handle the thermal noise, this implies a larger power consumption.

1.3 ADC Pipeline

The pipeline ADC has become the most popular ADC architecture for applications that require sampling rates from a few mega samples per second (MSps) up to 600 Msps, and resolutions range from eight bits at the faster sample rates up to 16 bits at the lower rates. These conversion frequences and resolutions cover a wide range of applications such as environmental monitoring, biomedical applications and telecommunication. For low sampling rates the successive approximation register (SAR) architecture, and oversampling/sigma-delta ADCs dominate the market. For higher sampling rates usually flash ADCs are used. Nonetheless, pipelined ADCs of various forms have improved greatly in speed, resolution, dynamic performance, and power consumption in recent years.

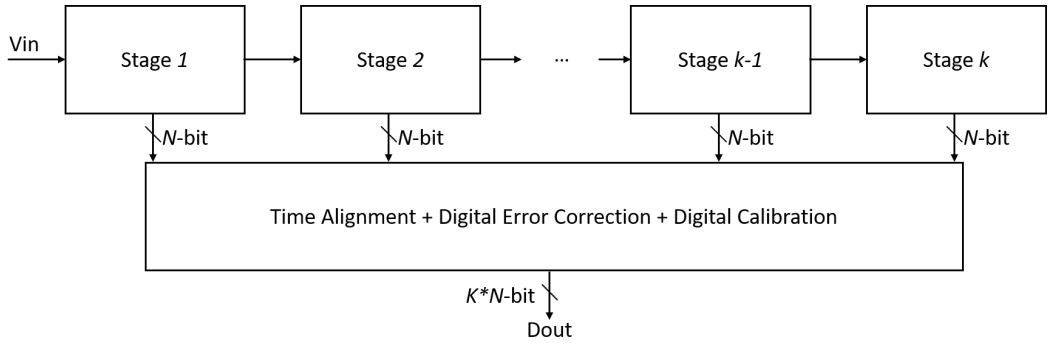

Figure 1.13. Block diagram of an ADC pipeline

In figure 1.13 a principle schematic of a pipelined ADC is shown. In each stage the analog input, Vin, is first sampled and held steady by a sample-and-hold structure, while the flash sub-ADC quantizes it in N bits (N bit is the number of conversion bit of each stage). The output of the sub-ADC is taken as input by the sub-DAC, and the analog output is subtracted from the input. This residue is the quantization error of the sub-ADC and then this signal is amplified by a factor 2^N and fed to the next stage. This gained-up residue continues through the pipeline, providing N bits

per stage until it reaches the last sub-ADC, which resolves the last N bits.

Because the bits from each stage are determined at different points in time, all the bits corresponding to the same sample are time-aligned with shift registers before being fed to the digital-error-correction logic. Note that when a stage finishes processing a sample, determining the bits, and passing the residue to the next stage, it can then start processing the next sample received from the sample-and-hold embedded within each stage. This pipelining action is the reason for the high throughput. The pipeline structure is affected by data latency, because each sample must propagate through the entire pipeline before all its associated bits are available for combining in the digital-error-correction logic.

1.3.1 Component Accuracy

Some errors such as gain error of error-amplifier or non-linearity in sub-DACs are not corrected by digital correction. The Sample-and-Hold at the beginning of the pipeline chain and the first stage's sub-DAC actually require the same accuracy of the whole ADC. The circuits in subsequent stages require less accuracy. This need for reduced accuracy is due to the fact that the later stages' error terms are divided down by the preceding interstage gain. The stages in the pipeline converter can be made progressively smaller to obtain a reduction in power consumption.

Usually, in pipelined ADCs, the Sample-and-Hold, sub-DAC, summation node, and gain amplifier are implemented as a single switched-capacitor circuit block called a multiplying DAC (MDAC). The major factor limiting MDAC accuracy is the intrinsic capacitor mismatch. In general, for about 12 bits of accuracy or higher, some form of capacitor/resistor trimming or digital calibration is required, especially for the first two stages.

1.3.2 The Multiplying DAC

The pipeline ADC is composed of several stages each with a low-resolution ADC, a DAC, and an error amplifier that generates the analog output signal. The output signal of the MDAC is

$$out_i = G_i \cdot (in_i - DAC_i) \tag{1.25}$$

where G_i is the gain of the MDAC, in_i the analog input and DAC_i the output of the DAC referred to the i-th stage. If $DAC_i = 0$ the MDAC behaves as a Sample-and-Hold amplifier, whereas if $in_i = 0$ it behaves as a DAC. Therefore the Sample-and-Hold and the DAC circuits can be considered as special cases of the MDAC and are not treated separately.

In literature different MDAC structures are available, in this work only the switching capacitors approach is considered. A common implementation of SC-

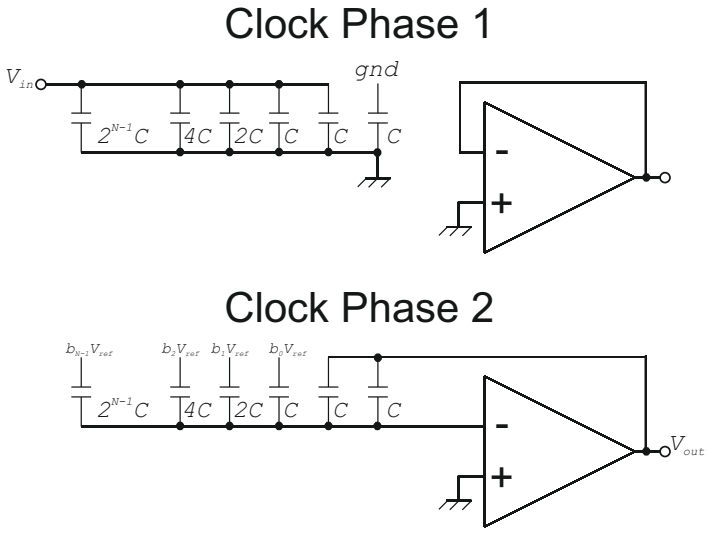

Figure 1.14. The SC MDAC of a pipeline converter

MDAC is shown in 1.14, it has N input bits $b_{n-1}, ..., b_0$, where b_{n-1} is the MSB and b_0 the LSB. A single bit of digital correction is used and then the residue gain is decreased by a factor 2. In the sampling phase ϕ_1, all capacitors except one are connected to the input voltage of the circuit, collecting the total charge on the top plates of the capacitors

$$q_s = V_{in} \cdot (2^{N-1}C + ... + C + C) \tag{1.26}$$

On the hold phase two of the capacitors are connected to the output, and the other are connected to the reference voltage $\pm V_{ref}$ according to the output of the sub-DAC. The total charge stored in this phase is

$$\begin{aligned} q_h = &\left(V_{out} + \frac{V_{out}}{A}\right) \cdot 2C + V_{ref} \cdot (2^{N-1} \cdot b_{N-1} \cdot C + ... + b_0 \cdot C) + \\ &+ \frac{V_{out}}{A} \cdot (2^{N-1}C + ... + C) + \frac{V_{out}}{A} \cdot C_p \end{aligned} \tag{1.27}$$

where A is the DC-gain of the opamp, C_p the parasitic capacitor, and $b_{N-1}, ..., b_0 = \pm 1$ are determined by the digital output of the sub-ADC. The total charge is conserved among the phases, then (1.26) is equal to (1.27) thus

$$V_{out} = \frac{V_{in} \cdot 2^{N-1} - \frac{V_{ref}}{2} \cdot (2^{N-1} \cdot b_{N-1} + ... + b_0)}{1 + \frac{C_{tot}}{2A_0C}} \tag{1.28}$$

the reference voltages in the DAC are $V_{ref-} = -\frac{FS}{2}$ and $V_{ref+} = \frac{FS}{2}$, where FS is the full-scale input range of the converter.

1.3.2.1 Effect of Finite Opamp Gain and Parasitic Capacitors

The non-ideality of the circuit such as finite opamp gain and parasitic capacitance, can affect the output voltage of the MDAC. From the first order Taylor expansion of (1.28) we get

$$\frac{1}{1+\epsilon} \approx 1-\epsilon \rightarrow \frac{1}{1+\frac{C_{tot}}{2A_0C}} \approx 1-\frac{C_{tot}}{2A_0C} \tag{1.29}$$

Thus the gain error is

$$\epsilon_G = \frac{C_{tot}}{2A_0C} = \frac{2^N+1+\frac{C_p}{C}}{2A_0} \approx \frac{2^{N-1}}{A_0} \tag{1.30}$$

this approximation is valid for large values of N. The gain error is the same for the input signal and sub-DAC output signal, therefore the gain error can be considered as an error at the output of the subtracter.

1.3.2.2 Effect of Mismatch

The residue of an MDAC stage is given by

$$V_{out} = \frac{\sum_1^{2^n} C_i}{C_f} V_{in} - \left[\frac{\sum_1^k C_i}{\sum_1^{2^n} C_i} V_{ref} - \frac{\sum_{k+1}^{2^n} C_i}{\sum_1^{2^n} C_i} V_{ref} \right] \tag{1.31}$$

if the values of $\sum_1^{2^n} C_i$ and C_f are different, the transcharateristic of the MDAC will be affected by gain error. The mismatch between sampling capacitors, C_i also affects the linearity of the DAC. The mismatch between two capacitors is determined by the area of a capacitor

$$mismatch \propto \frac{1}{\sqrt{capacitor\ area}} \tag{1.32}$$

Thus, to achieve an high linear ADC, large capacitors are required to minimize the effect due to capacitor mismatch. Commonly, during the design of the MDAC the value of capacitors is not set by the thermal noise requirement, but the high linearity requirements sets a lower bound on the value of capacitors to suppress the effect of mismatch. The layout of the MDAC should be done using design techniques that improves the capacitor matching, such as using arrays of unit size capacitors in a highly symmetric configuration, and use dummy capacitors around the periphery of the array to overcome the fringe effect [2]. An arbitrarily high level of matching cannot be achieved using good layout techniques alone, hence limiting pipelined ADC resolution to the medium-high range as shown in figure 1.1. A typical solution is to use digital calibration techniques as discuss in chapter 3.

1.3.2.3 Speed

Under the single pole condition, the settling of the output of the opamp is linear, and the error due to finite settling time ϵ_r is described by

$$\epsilon_r = e^{-t_s \cdot \omega_{-3dB}} \tag{1.33}$$

where t_s is the settling time, and ω_{-3dB} is the bandwidth of the opamp. Settling error causes a finite gain error on the output signal of MDAC. The maximum settling time is half of the sampling period $1/f_s$. Considering the unity-gain bandwidth ω_u as

$$\omega_u = \frac{\omega_{-3dB}}{\beta} \tag{1.34}$$

that for a single stage opamp is $\omega_u = g_m/C_{load}$. In the previous expression β is the feedback factor that is equal to

$$\beta = \frac{2C}{(2^N+1)C + C_p} = \frac{2}{(2^N+1) + C/C_p} \tag{1.35}$$

The capacitive load for a single stage is

$$C_{load} = \beta \cdot ((2^N - 1)C + C_p) + C_{next} \tag{1.36}$$

where C_{next} is the capacitive load of the next stage. Under the hypothesis of identical stages, and for large number of stages N, the (1.36) becomes

$$C_{load} = \beta \cdot ((2^N - 1)C + C_p) + 2^N C \approx 2^N C \tag{1.37}$$

The maximum speed of the MDAC can be calculated as

$$f_s = \frac{1}{2t_s} = \frac{\omega_{-3dB}}{2ln(1/\epsilon_r)} = \frac{\omega_u \cdot \beta}{2ln(1/\epsilon_r)} = \frac{\frac{g_m}{2^N C} \cdot \frac{2}{(2^N+1)+C_p/C}}{2ln(1/\epsilon_r)} \tag{1.38}$$

that can be approximated with

$$f_s \simeq \frac{g_m}{2^{2N} C \cdot ln(1/\epsilon_r)} \tag{1.39}$$

For low gain or large β the linear settling assumption is not valid, and the settling will restricted by slew rate, and the settling time is increased if compared with (1.39).

1.3.3 subADC

The subADC in i-th stage is assumed to have output code $D_{out}(i)$, that is an integer number ranging from 0 to $N_i - 1$, and can be calculated as

$$D_{out}(i) = \sum_{l=0}^{n_i - 1} b_{i,l} \cdot 2^l \tag{1.40}$$

where $b_{i,l}$ is the l-th output bit of the i-th stage. We assume that the input signal range from $-FS/2$ to $+FS/2$ and that the threshold levels are equally spaced over the entire input range as shown in figure 1.15

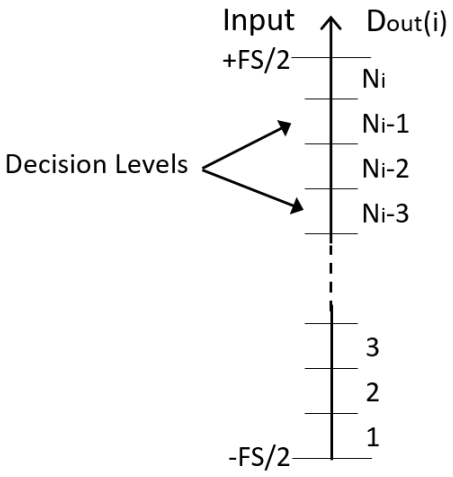

Figure 1.15. The input dynamic is divided in 2^N levels

Figure 1.15 shows the input range subdivided N_i times, where each segment corresponds to one output code. The analog value corresponding to one LSB is

$$LSB_i = \frac{FS}{N_i} \tag{1.41}$$

1.3.4 subDAC

The analog output of the subDAC for a certain code is determined by the expression

$$V_{dac}(i) = \left(D_{out}(i) - \frac{N_i - 1}{2}\right) \cdot \frac{FS}{N_i} \tag{1.42}$$

1.3.5 Sample-and-Hold and Residue Amplifier

In a pipeline stage, the difference between the analog input and the DAC output is the residue

$$V_{res}(i) = V_{in}(i) - V_{dac}(i) = V_{in}(i) - \left(D_{out}(i) - \frac{N_i - 1}{2}\right) \cdot \frac{FS}{N_i} \tag{1.43}$$

Figure 1.16 shows the tranfer function of the subtractor. The output swing is N_i times smaller than its input. It is therefore necessary to amplify the residue in order to utilize the entire rampe of the following stage. The analog output of one stage can be calculated by

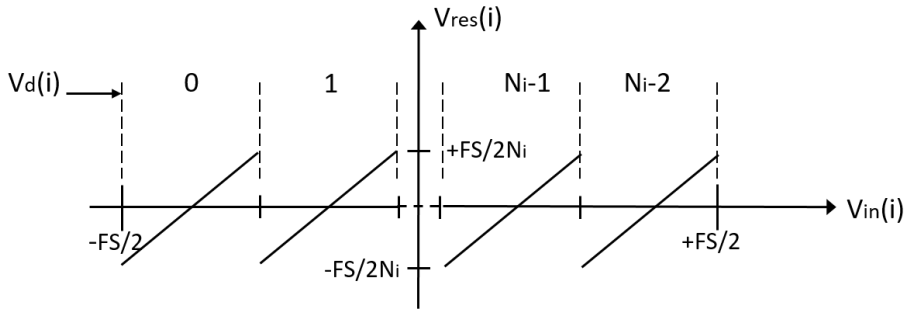

Figure 1.16. Transfer function of an N-bit MDAC

$$V_{out}(i) = V_{res}(i) \cdot G_i = \left[V_{in}(i) - \left(D_{out}(i) - \frac{N_i - 1}{2}\right) \cdot \frac{FS}{N_i}\right] \cdot G_i \tag{1.44}$$

Choosing the signal swing equal in each stage, and the gain as N_i, the output signal can be written as

$$V_{out}(i) = \left[V_{in}(i) - \left(D_{out}(i) - \frac{N_i - 1}{2}\right) \cdot \frac{FS}{N_i}\right] \cdot N_i \tag{1.45}$$

1.3.6 Digital Output Recostruction

The digital outputs of all stages must be combined to generate the total output code.

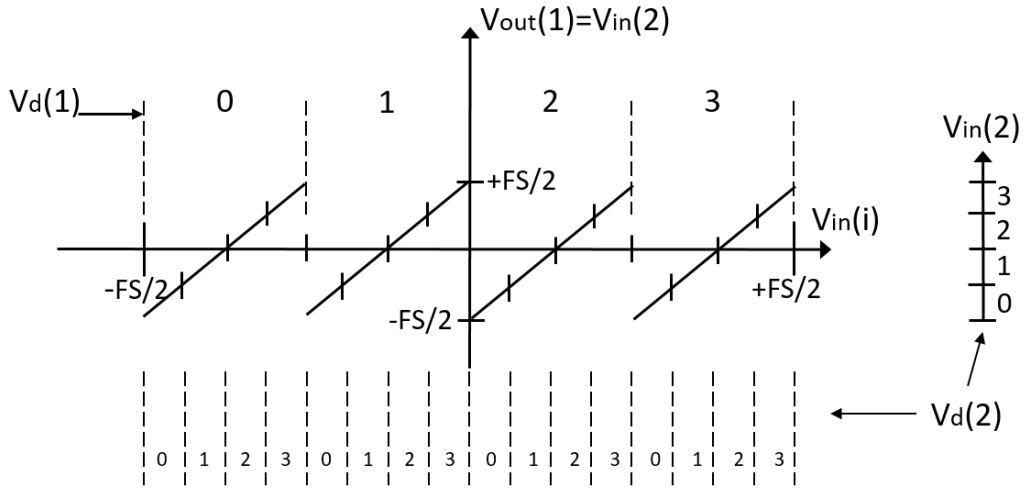

Figure 1.17. Analog output of first stage and corresponding digital output codes of a two stage ADC

As shown in figure 1.17 the output signal of i-th stage feeds the next stage, hence each segment of the sawtooth-shaped output signal of the i-th stage will be

quantized by the $i+1$-th stage. The number of codes in a pipelined ADC where $G_i = N_i$ can be calculated as

$$N_{tot} = \prod_{i=1}^{m} N_i \tag{1.46}$$

if all resolutions are choosen as $N_i = 2^{n_i}$ the total number of bits is given by

$$n_{tot} = \prod_{i=1}^{m} n_i \tag{1.47}$$

using the (1.44) the input signal of the first stage can be written as

$$V_{in}(1) = V_{dac}(1) + \frac{V_{out}(1)}{G_1} \tag{1.48}$$

since $V_{in}(2) = V_{out}(1)$ we can use again (1.44) to get

$$V_{in}(1) = V_{dac}(1) + \frac{V_{dac}(2)}{G_1} + \frac{V_{out}(2)}{G_1 \cdot G_2} \tag{1.49}$$

repeating iteratively for all the stages we get

$$V_{in}(1) = V_{dac}(1) + \frac{V_{dac}(2)}{G_1} + \cdots + \frac{V_{dac}(i)}{G_1 \cdots G_{i-1}} + \cdots + \frac{V_{dac}(m)}{G_1 \cdots G_{m-1}} + V_{res}(m) \tag{1.50}$$

the residue of the last stage $V_{res}(m)$ corresponds to the quantization error of the converter. Using (1.42) and (1.50) we get

$$V_{in}(1) = \sum_{i=1}^{m} \left[\left(D_{out}(i) - \frac{N_i - 1}{2} \right) \cdot \frac{FS}{N_i} \cdot \frac{1}{\prod_{k=1}^{i-1} G_k} \right] + V_{res}(m) \tag{1.51}$$

The total output code of a converter is

$$D_{out} = \sum_{i=1}^{m} \left(D_{out}(i) \cdot \frac{N_m}{N_i} \cdot \prod_{k=i}^{m-1} G_k \right) \tag{1.52}$$

when $G_k = N_i$, (1.52) becomes

$$D_{out} = \sum_{i=1}^{m} \left(D_{out}(i) \cdot \prod_{k=i+1}^{m} N_k \right) \tag{1.53}$$

1.3.7 Digital Error Correction

To reduce the accuracy requirement of the sub-ADC and sub-DAC, the pipeline ADCs employs a technique called "digital error correction". In a pipeline ADC the main issue is due to the offset in the sub-ADC, because, if one of the comparators in the first N-bit flash ADC has a significant offset, its threshold is moved, as shown in figure 1.18. Thus, when an analog input is close to the trip point, an incorrect

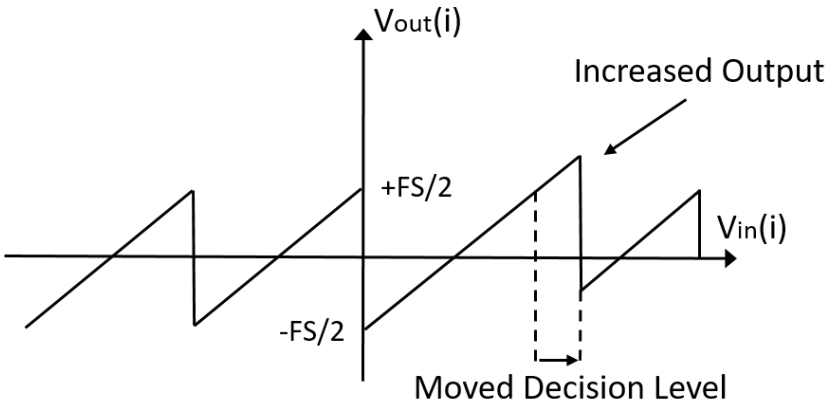

Figure 1.18. Moved ADC decision level increases signal swing.

code is provided to sub-DAC, consequently an incorrect DAC output would result, that produces a wrong residue.

As long as the amplified residue does not saturate the subsequent stage, the LSB code generated by the remaining pipeline will give the correct ADC output code. Much smaller is the residue gain, and more larger is the acceptable error. The maximum decision deviation is given by

$$\Delta V = \pm \frac{FS}{2} \left(\frac{1}{G_i} - \frac{1}{N_i} \right) \tag{1.54}$$

if the residue gain is 2 the decision deviation become

$$\Delta V = \pm \frac{FS}{2N_i} \tag{1.55}$$

Hence, the error in ADC_i can be $\pm LSB_1/2$, without causing a large conversion error. The implication is that none of the sub-ADCs has to be accurate as the entire ADC. In fact, the sub-ADC in each stage requires only N bits of accuracy.

1.4 MDAC Implementation

Splitting the conversion in a pipeline chain allows an optimization of the conversion speed respect to the speed of the used circuit. The first stage need the maximum accuracy, the latter stages can be designed with reduced accuracy without influencing the overall resolution. Different architectures can be used to achieve the required resolution. In this section different architecture will be discussed.

1.4.1 1 bit MDAC

The implementation of 1-bit MDAC is shown in figure 1.19 , and the transfer function is reported in figure 1.20. As shown the subADC is reduced to a zero crossing comparator.

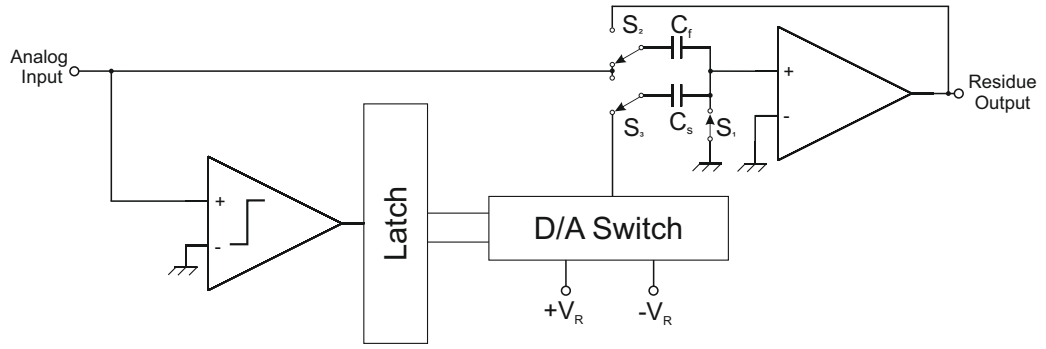

Figure 1.19. Single bit MDAC

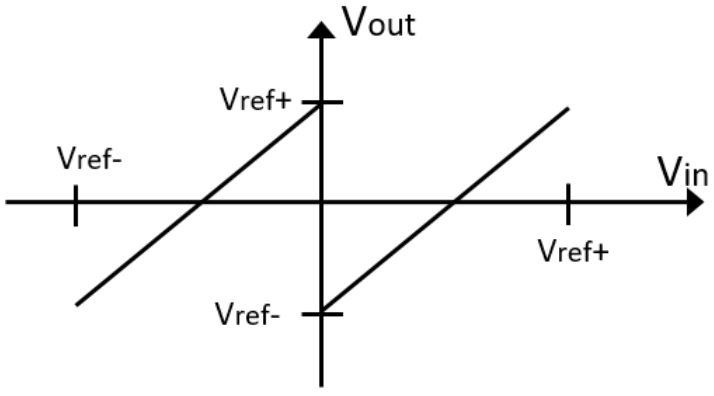

Figure 1.20. 1-bit residue signal

The result of the comparation drives the sub DAC, that is a switch that connects $+V_R$ or $-V_R$ to the subtractor. During the sampling phase switch S_1 is closed and

switches S_2 and S_3 connects the analog input to the sampling capacitors to store the analog input. During the next phase, S_1 is opened, and S_2 connect the capacitor C_2 between the input and the output of the opamp. Switch S_3 connects the capacitor C_1 to the subDAC. During this phase the reference voltage V_R is added or subtracted to the analog input signal. The analog output result is stored on the capacitor C_2. Under the condition of charge conservation between the two phases, the output voltage can be written as

$$V_{out} = \left(1 + \frac{C_1}{C_2}\right) \cdot V_{in} + D \cdot V_R \tag{1.56}$$

where D is the output data of the subADC and has value ± 1. Choosing $C_1 = C_2$ then a gain of 2 is obtained. The matching between the two capacitors is a keypoint to determine the accuracy. Figure1.20 shows the ideal tranfer function of the 1-bit MDAC. When the circuit is affected by offset or the gain is larger than 2, the following stage is fed with an error affected signal.

1.4.2 1.5 bit MDAC

An improvement of this MDAC structure is the 1.5-bit MDAC.

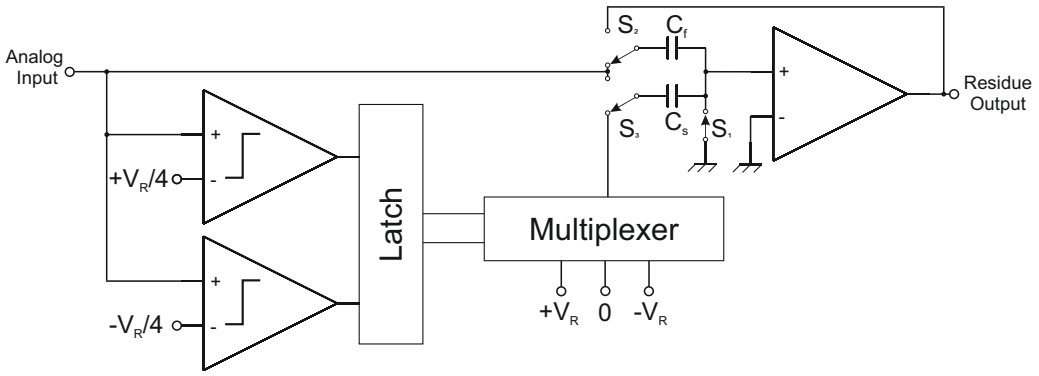

Figure 1.21. 1.5 bit MDAC implementation

As shown in figure 1.21 the subADC in this structure has 2 levels that are set on $+\frac{V_r}{4}$ and $-\frac{V_r}{4}$. The subDAC consists of a three-level multiplexer with reference voltages $+V_R$, 0 and $-V_R$. During the sampling phase the switch S_1 is closed to ground and through S_2 and S_3 the input signal is stored on the capacitors C_s and C_f. During the next phase called "error amplification phase" the operation performed depends on the data of the subADC

$$V_{residue} = \begin{cases} \left(1 + \frac{C_s}{C_f}\right) V_{in} - V_R, & \text{if } V_{in} > \frac{V_R}{4} \\ \left(1 + \frac{C_s}{C_f}\right) V_{in}, & \text{if } -\frac{V_R}{4} < V_{in} < +\frac{V_R}{4} \\ \left(1 + \frac{C_s}{C_f}\right) V_{in} + V_R, & \text{if } V_{in} > -\frac{V_R}{4} \end{cases} \tag{1.57}$$

In this phase the switch S_1 is open, and the capacitor C_f is connected as a feedback element over the opamp, while capacitor C_s is connected at the output of the subDAC. Also in this architecture the capacitors C_s and C_f are equal to set the gain of the stage exactly to 2x.

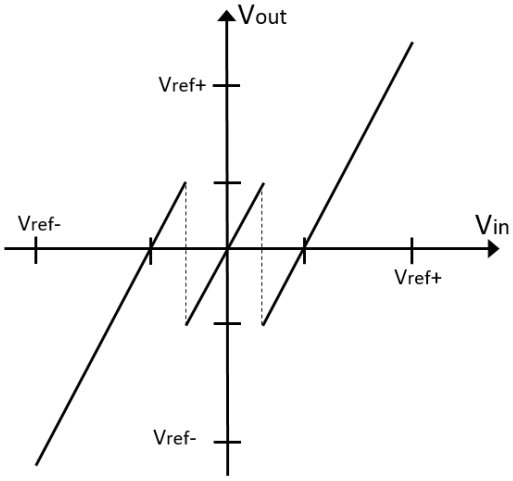

Figure 1.22. 1.5-bit residue signal

The transfer function of this stage is reported in figure 1.22. The 2 level ADC in this system enables correction of signal errors due to non exact gain, offset and switch charge transfer. In a piplined ADC with digital correction the residue gain is reduced to introduce redundancy.

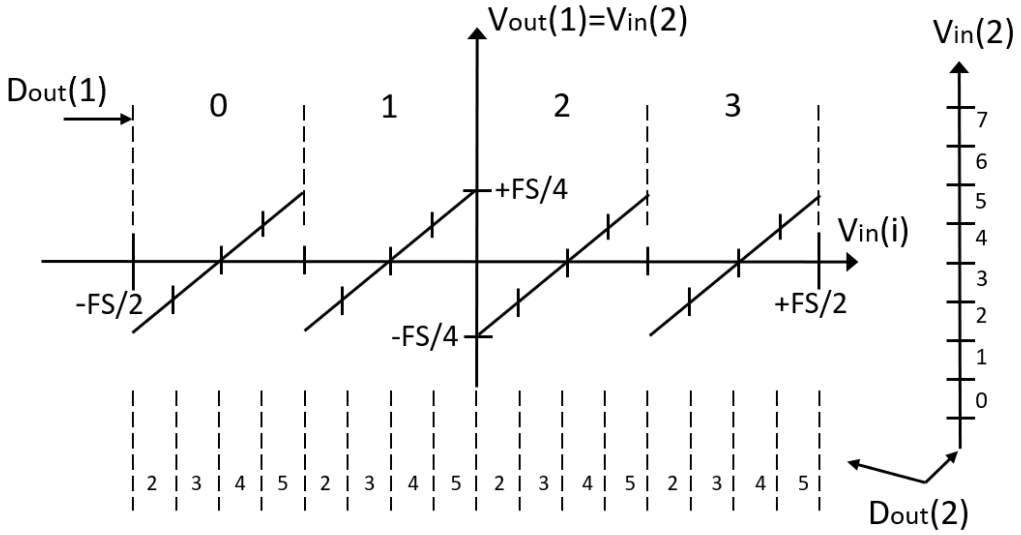

Figure 1.23. Analog output of the first stage and corresponding digital output codes for a two stage ADC with reduced residue gain.

Figure 1.23 illustrate for a two stage ADC, where the first stage has 4 codes

and the second stage has 8 codes. The residue gain has been reduced from 4 to 2. The output signal swing of the first stage is now only half the input range of the following stage. This means that the codes 0,1,6 and 7 will never be used. The gain is usually reduced by a factor 2 but can in principle be chosen arbitrarily. However, it is usually desirable to have the same step size for all the codes. The gain is then restricted to values that give the correct step size at the decision levels in the first stage.

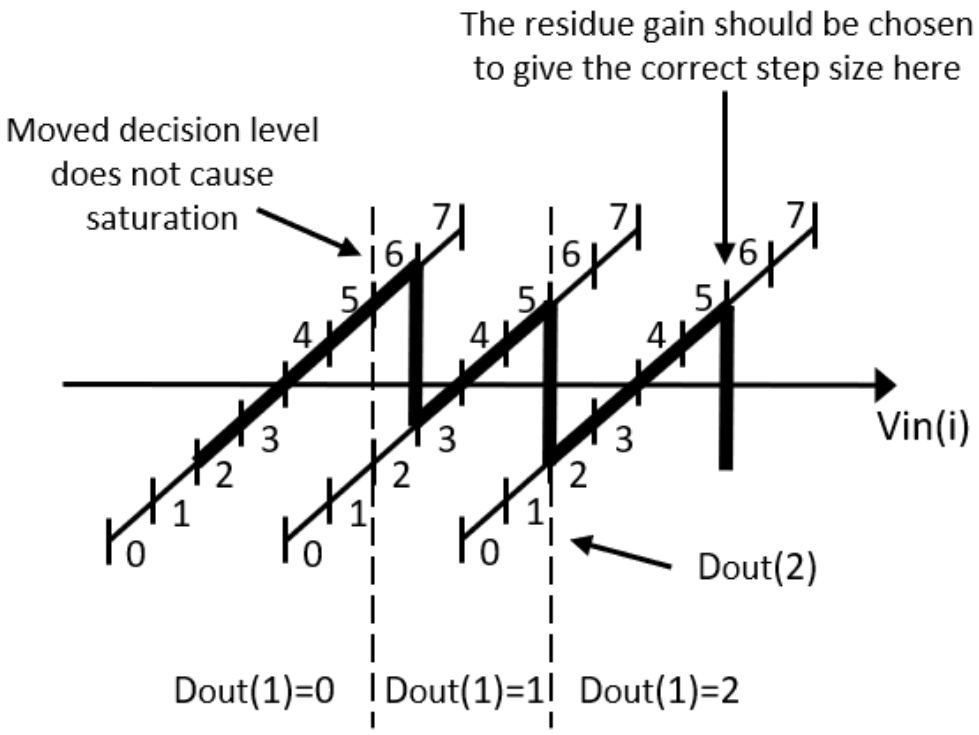

Figure 1.24. A moved decision line does not cause saturation in the following stage when the residue gain is reduced.

Figure 1.24 shows the output when one of the decision lines has been moved. In this figure it is seen that moving the decision level will not cause saturation in the following stage since there are now the redundant codes **0, 1** and **6, 7** in stage 2. The digital correction can correct errors in the comparators as long as the residue is within the FS range of the following stage. The smaller the residue gain, the larger errors can be accepted. The maximum decision line deviation is given by

$$\Delta V = \pm \frac{FS}{2} \left(\frac{1}{G_i} \frac{1}{N_i} \right) \tag{1.58}$$

If the gain factor is reduced by a factor 2 we get

$$\Delta V = \pm \frac{FS}{2N_i} \tag{1.59}$$

Hence the error in the ADC_i can be $\pm LSB_i/2$, without causing a large conversionerror. A drawback of the digital correction is, as was illustrated by the example above, that several code combinations give the same total output code. The total resolution of the converter is thus decreased when digital correction is introduced unless more stage are added.

1.4.3 Multi bit MDAC

Usually pipeline ADCs with more than 12 bit resolution use at the first stage a multi-bit quantizer. Then the ADC is completed with 1.5 bit stages.

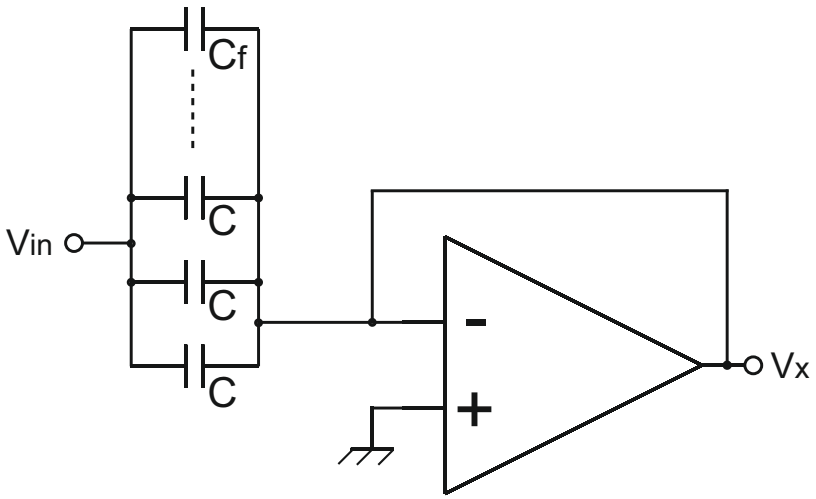

Figure 1.25. Multi-bit MDAC during the sampling phase

The multi-bit ADC consists of N level subADC and subDAC, and a Sample-and-Hold with gain equal to N. To obtain the maximum accuracy in the system all the capacitors of the Sample-and-Hold have the same size. The feedback capacitor is made equal to the subDAC capacitor. During the sampling phase the input signal is sampled on all the capacitors as shown in figure 1.25. During the next phase when the subtraction and amplification are performed, the residue is calculated using the data provided by the sub-ADC. Depending on the value of the bits the reference voltage V_{ref} is added or subtracted. The equivalent circuit of a multi bit MDAC during the error amplification phase is shown in figure 1.26.

Depending on the configuration of the bits provided by the subADC a subtraction or an addition with V_{ref} is performed. Figure 1.27 shows the transfer function of the multi-stage MDAC.

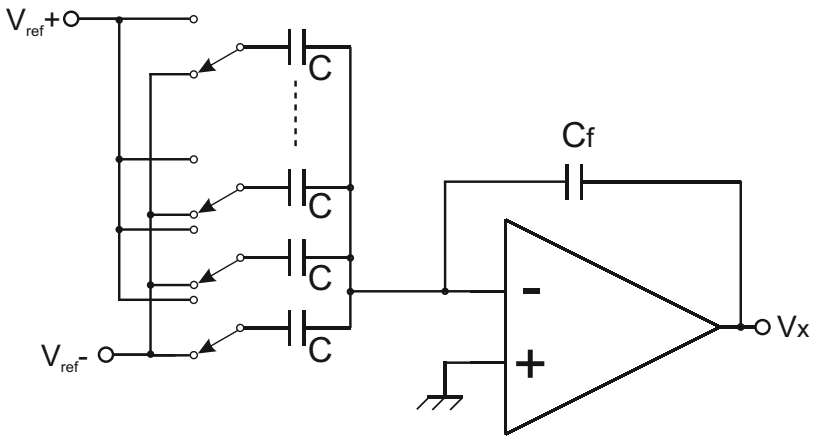

Figure 1.26. Multi-bit MDAC during the error amplification phase.

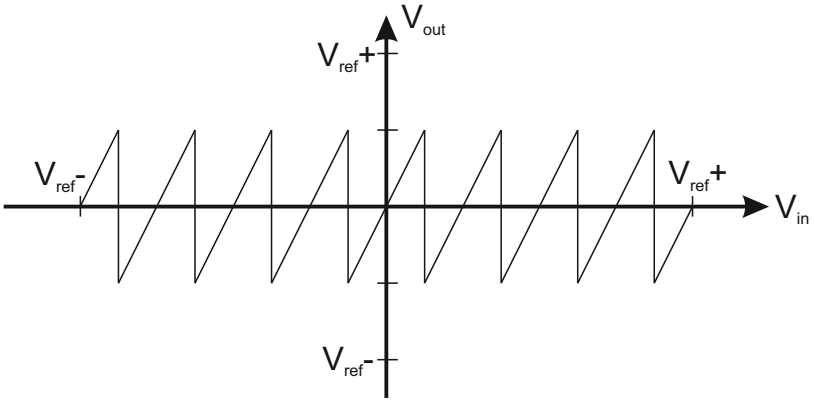

Figure 1.27. Multi-bit residue signal

1.5 Issues in Pipeline ADC

Previously some generic errors which may occour in ADC has been discussed. Some issues are associated to specific ADC's implementation, thus are described separately in this section.

1.5.1 Noise in MDACs

In CMOS circuits there are two fundamental kinds of noise: the thermal noise and the flicker noise. the statistical characteristics of noise processes are different as the frequency behaviour, in fact, the thermal noise is white, while the flicker noise is frequency dependent ($1/f$). The flicker noise is dominant at low frequency, while for higher frequencies is neglectable. Also, the flicker noise can be decreased using circuital techniques such as the correlated double sampling, therefore, the flicker noise can be neglect in the following.

1.5.1.1 kT/C

The switches employed in switched-capacitor circuits generate thermal noise, that is integrated into the sampling capacitor with a bandwidth of $f_s/2$, where f_s is the switching frequency. The total power is kT/C, and is independent of the r_{on} resistance of the switch [3]. The noise in the bandwidth is

$$v_{n,C}^2 = \frac{k \cdot T}{C} \cdot \frac{BW_S}{f_s/2} = \frac{k \cdot T}{C} \cdot \frac{1}{OSR} \tag{1.60}$$

where k is the Boltzmann's constant, T is the absolute temperature, C the sampling capacitor, BW_S the bandwidth of the signal, f_s the sampling frequency and OSR the oversampling ratio. In the fully differential circuits, the noise is integrated into both the positive and negative sampling capacitors, and the bandwidth is doubled if compared with (1.60). However, also the signal swing is doubled in fully differential architectures, and therefore the dynamic range is improved by 3dB.

1.5.1.2 Thermal Noise in Opamp

If we consider a single stage opamp, the input referred noise power spectral density is given by

$$S_{n,amp}(f) = 2 \cdot \frac{8}{3} \cdot \frac{kT}{g_m} \cdot (1 + n_t) \tag{1.61}$$

where g_m is the transconductance of the input transistor and n_t is the thermal noise. Equation (1.61) shows that increasing the transconductance gives a reduction of the spectral density of power noise, but it can be hard to reach. Otherwise, we can reduce the noise contribution factor by choosing an opamp structure with a better noise figure.

1.5.2 Thermal Noise in SC-MDAC

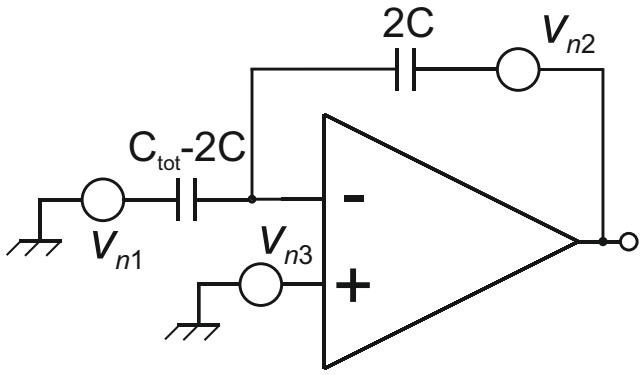

Figure 1.28. Noise sources during the error amplification phase

In figure 1.28 we assume the opamp ideal in terms of gain, input/output impedances and neglect the parasitic capacitors. Consider the thermal noise of the switches and the opamp, in the sampling phase only the noise of the switches should be considered

$$v_n^2 = \frac{kT}{(2^N+1)\cdot C} = \frac{kT}{C_{tot}} \tag{1.62}$$

where C_{tot} is the total capacitance in the MDAC. The total noise charge is

$$q^2 = \frac{kT}{C_{tot}} \cdot C_{tot}^2 = kT \cdot (2^n+1) \cdot C \tag{1.63}$$

during the hold phase this charge is converted to a voltage, thus the total voltage noise referred to the output of the MDAC, generated in sampling phase is

$$v_{n,sample}^2 = \frac{q^2}{(2C)^2} = \frac{kT \cdot (2^N+1)}{4C} \tag{1.64}$$

that for large N becomes

$$v_{n,sample}^2 \approx \frac{kT}{C} \cdot 2^{N-2} \tag{1.65}$$

Where v_{n1} and v_{n2} represent the thermal noise of the switch, and v_{n3} represents the thermal noise of the opamp. In this phase the noise contribution from a noise source can be calculated as

$$v_{out,k}^2 = S_k(f) \cdot |H_k|^2 \cdot BW_{N,k}, \quad k = 1,2,3 \tag{1.66}$$

where $S_k(f)$ is the spectral density of the noise source k, $|H_k|$ the gain from the k-th noise source to the output, and $BW_{N,k}$ the bandwidth (that is equal to $\frac{\beta\cdot\omega_u}{4}$

for all the considered noise sources). The gain from each noise source is

$$\begin{aligned} |H_1| &= \frac{C_{tot} - 2C}{2C} \\ |H_2| &= 1 \\ |H_3| &= \frac{C_{tot}}{2C} \end{aligned} \tag{1.67}$$

and the spectral densities are

$$\begin{aligned} S_1(f) &= 4kT \cdot R_1 \\ S_2(f) &= 4kT \cdot R_2 \\ S_3(f) &= 2 \cdot \frac{8kT}{3g_m} \cdot (1 + n_t) \end{aligned} \tag{1.68}$$

where R_1 and R_2 are the resistances of the switches when they are in on state. Usually the R_{ON} of the switches is lower than $1/g_m$, and in this case the noise of the ompamp will dominate, and we have

$$v_{n,hold}^2 = \frac{16}{3}\frac{kT}{g_m} \cdot \left(\frac{C_{tot}}{2C}\right)^2 \cdot \frac{\beta \cdot \omega_u}{4} \cdot (1 + n_t) \tag{1.69}$$

The transconductance g_m and the capacitive load C_{tot} determine the unity-gain bandwidth ω_u. Hence we have

$$\begin{aligned} v_{n,hold}^2 =& \frac{16}{3}\frac{kT}{g_m} \cdot \left(\frac{C_{tot}}{2C}\right)^2 \cdot \frac{\beta \cdot \frac{g_m}{C_{load}}}{4} \cdot (1 + n_t) = \\ &= \frac{16}{3} kT \cdot \left(\frac{2^N + 1}{2}\right)^2 \cdot \frac{\frac{2}{2^N+1}}{4C_{load}} \cdot (1 + n_t) = \\ &= \frac{2}{3}\frac{kT}{C_{load}} \cdot (2^N + 1) \cdot (1 + n_t) \end{aligned} \tag{1.70}$$

The total noise at the output is due to the sum of noise contributions in both the sample and hold phases

$$v_{tot}^2 = v_{n,sample}^2 + v_{n,hold}^2 \quad \approx \quad \frac{kT}{C} \cdot 2^{N-2} + \frac{2}{3}\frac{kT}{C_{load}} \cdot (2^N + 1) \cdot (1 + n_t) \tag{1.71}$$

If the load capacitance is the same order of sampling capacitor, the noise is dominated by $v_{n,sample}^2$ in the sampling capacitors. In this case the input referred noise of the MDAC is given by

$$v_{tot,in}^2 = \frac{kT}{C} \cdot \frac{2^N - 2}{(2^N - 2)^2} = \frac{kT}{2^N C} \approx \frac{kT}{C_{tot}} \tag{1.72}$$

It should be noted that the total noise depends only on the capacitors in the circuit, while it is independent by g_m.

1.5.2.1 Distortion Model for Pipeline ADCs

Several error sources are present in ADC pipeline, which limit maximum achievable linearity. Some error sources, such as comparator offset, can be effectively counteracted through the use of particular techniques such as digital redundancy, using 1.5-bit MDAC stages. Other error sources such as capacitor mismatch and finite gain error cannot be addressed in this way, and are the main limitations of linearity in these ADCs. The need of high gain amplifiers limits the maximum achievable conversion rate, while the need of well matched capacitors increases their size, with subsequent large chip area and power consumption. For a N stages pipeline ADC the ideal behaviour of the K-th stage can be described as

$$V_{O,K} = 2V_{I,K} - D_K \tag{1.73}$$

where $V_{O,K}$ is the output voltage of the stage and $V_{I,K}$ is the input voltage, and D_K is the stage digital input, wich is given by:

$$D_K = \begin{cases} 1, & \text{if } V_{I_K} > 1/4 \\ -1, & \text{if } V_{I_K} < 1/4 \\ 0, & \text{otherwise} \end{cases} \tag{1.74}$$

where the reference voltage has been normalized to 1. In non-ideal MDACs, effects such as finite amplifier gain and capacitor mismatch change the slope of the transfer curve. The input/output characteristic of the K-th MDAC can be described [4] by two error parameters, named α_K and β_K obtaining the expression:

$$V_{O,K} = 2(1+\alpha_K)V_{I,K} - (1+\beta_K)D_K \tag{1.75}$$

considering also the capacitor mismatch $\epsilon = \Delta C/C$ and finite gain Av of opamp, α_K and β_K becomes:

$$\alpha_K = \frac{1+\epsilon/2}{1+\frac{2+\epsilon}{Av}} - 1 \; ; \; \beta_K = \frac{1+\epsilon}{1+\frac{2+\epsilon}{Av}} - 1 \tag{1.76}$$

Moreover, these error parameters can also be used to describe the effect of finite settling time, amplifier input capacitance and of the error on the reference voltage.

A non-ideal ADC can be described by two error vectors $\alpha = \{\alpha_1, \alpha_2, \cdots, \alpha_{Nb-1}\}$, and $\beta = \{\beta_1, \beta_2, \cdots, \beta_{Nb-1}\}$ which give the two error parameters for each stage. An ideal converter obviously has all-zero error vectors.

Given the input signal V_I , an ideal converter will give $N_b - 1$ output codes ideal D_K . On the other hand, the real converter will give output codes D_K. The reconstructed output signal will be, respectively:

$$V_O^{ideal} = \sum_{K=1}^{N_b-1} \frac{D_K^{ideal}}{2^K} \text{ and } V_O^{real} = \sum_{K=1}^{N_b-1} \frac{D_K^{real}}{2^K} \tag{1.77}$$

The input of the K-th stage will be named $V_{I,K}$ and ideal $V_{I,K}$, for the real and ideal converter, respectively. The ratio between the power of V_I and the power of the difference between V_I and V_O gives the THD. In the ideal ADC, the quantization error sets a minimum level for THD. Anyway, error sources can decrease linear performance even further in the non-ideal ADC. The error sources in different MDAC stages interact in a non-linear way: errors cannot be simply added together, because errors in the previous stages will affect the inputs of the following ones.

The contribution of each stage to overall error is supposed to be ideal ideal $V_{err,K} = 2\alpha_K V_{I,K}^{ideal} - \beta_K D_K^{ideal}$, which is the difference between the output of the ideal and the actual MDAC stages, given the same input signal. By reporting this error to the input, is possible compute the effect of each non-ideality on linearity, for a certain input signal V_I. The output of the last stage is the quantization error, which would be present also in the ideal converter. A complete distortion model for pipeline ADC is described in [5]

1.6 Figures of Merit of ADCs

The choice between different converters is driven by different criteria, first of all the converter performance must fit the system requirement as the ENOB and sampling frequency. Moreover in low power applications also the energy efficiency of a converter plays a keyrole, thus a figure of merit that describes the power efficiency must be defined. The combination of bandwidth, power and accuracy defines a figure of merits (FOM), and allows to compare different designs. The energy efficiency of a data converter is defined through its Energy per Sample (ES), the dependence ES vs. ENOB (Effective Number Of Bits) is defined in an area bounded by two straight lines: the FOM of Walden (FOM_W) and the Thermal FOM (FOM_T). The two figures of merit (defined below), are used under different conditions: the FOM_W is used when the performance is limited by distortions, while FOM_T is used when the thermal noise is dominant. The Walden FOM (1.78) says that the energy ES doubles for each additional ENOB bit:

$$FOM_W = \frac{P_{diss}}{F_s 2^{ENOB}} \tag{1.78}$$

The thermal FOM (1.79) say that the energy ES quadruples every additional ENOB bit:

$$FOM_T = \frac{P_{diss}}{F_s 2^{2ENOB}} \tag{1.79}$$

The 1.78 show that an ADC is optimised respect the energy per sample. In fact, this figure-of-merit displays a strong correlation with many design parameters.

The relation between the actual power consumed by the circuit P_{circ} and the minimum power level of the signal needed to overcome the thermal noise with a

certain SNR $P_{sig,min} = 4kT \cdot BW \cdot SNR$ can also be used to define the power efficiency as:

$$\eta = \frac{P_{circ}}{P_{sig,min}} = \frac{P_{circ}}{4kT \cdot BW \cdot SNR} \tag{1.80}$$

This relation is often used to evaluate the efficiency of filters, opamps, etc. This relation is also the basis for the "Schreier Figure of Merit" for analog-to-digital converters :

$$FOM_S = 10Log_{10}\frac{SNR \cdot BW}{P_{ADC}} = SNR\_dB \tag{1.81}$$

The idea behind this Figure of Merit is that a better SNR requires proportionally lower thermal kT/C noise, leading to proportionally higher capacitor values, that need to be charged with proportionally larger currents. So the power follows the SNR and the FOM_S remains the same. This allows comparing converters with different specifications and is a basis to judge the design quality.

1.7 State of the Art of Pipeline ADCs

In recent years, low-power, moderate-resolution and moderate speed ADCs are gathering attention in many electronic applications. Among them, pipeline ADCs have been widely used, in table 1.3 are summarized the literature solutions with the best FOMs for low-voltage pipeline ADC implemented in short channel technologies.

Year	Architecture	Technology	Author	P[mW]	f_s[MHz]	$FOM_W \left[\frac{fJ}{conv}\right]$
2013	Pipe, TI	0,028	J. Wu	500	5400	101,0
2013	Pipe	0,18	B. Hershberg	2,96	20	-
2013	Pipe	0,13	T. Oh	6,38	70	38,2
2013	Pipe	0,065	N. Dolev	11,5	200	39,6
2013	Pipe	0,065	Shiuh-hua	19	800	51,7
2013	Pipe	0,028	B. Verbruggen	2,14	410	6,4
2014	Pipe	0,18	H. Venkatram	6	30	47,7
2014	Pipe, SAR, TI	0,028	B. Verbruggen	2,3	200	4,4
2014	Pipe, SAR	0,065	C. Lin	5,3	210	20,7
2014	Pipe, SAR	0,04	Y. Zhou	4,96	160	17,5
2016	Pipe, SAR, TI	0,028	Yuan-C. Lien	14,6	800	17,3
2016	Pipe, TI	0,028	Ahmed M.A.	2300	5000	398,5
2017	Pipe, SAR, TI	0,016	E. Martens	3,6	303	5,0
2017	Pipe	0,028	K.-J. Moon	6	500	21,5
2017	Pipe	0,028	J. Lagos	14,2	600	36,0
2017	Pipe, SAR	0,04	Y. Lim	2,3	100	-
2017	SAR, Pipe	0,18	D. Hummerston	11,4	2	-

Table 1.3. Literature survey on ADC pipeline

Note that pipeline ADC require several opamps and numerous comparators, wich result in large power dissipation. Besides, SAR ADCs are favored due to their simple structure and high power efficiency, but their conversion speedis largely limited by serial decision processes, and also the area increases with the resolution. In many applications which require higher-performance ADCs, the above conventional structures (pipeline ADCs and SAR ADCs) could not meet the system requirement completely. The perfect trade-off among speed, power, and linearity, is reached by hybrid structure of pipelined SAR ADCs, which is composed of pipeline ADC and SAR ADC [6], [7], [8] . In a pipeline ADC, larger first stage MDAC resolution improves the overall ADC linearity and relaxes noise and matching requirements, because the errors from the later stages are divided by the large inter-stage gain. However, larger first stage MDAC resolution exponentially increases the area and power of the first stage MDAC because of the flash sub-ADC. Therefore, in the pipelined SAR structure, the flash sub-ADCs are replaced by SAR ADC, which

makes the high-resolution MDAC possible. In addition, the sub-SAR ADC, which halves in resolution, also has a better performance in speed and area compared with a SAR ADC.

The main factors that mostly affect the performance of pipelined ADC are the errors related to the shift of the threshold voltage of the sub-ADC involved in the single stages, and also the non idealities in the sub-DAC. The latter one error can be due to many causes, such as offset, finite gain error, non-linearity and incomplete settling. In particular, the most limiting factors for accuracy are the mismatch between the sampling capacitors, the offset and the noise in the circuit. Moreover the limitations for the energy efficiency are given by the accuracy constraints, in fact, for a certain conversion frequency, results a requirement on the bandwidth and on the gain of the OPA (Operational Amplifier). The gain and the bandwidth and also other properties of an opamp are strictly related to the quiescent current, thus for a given set of constraints a lower limit on the quiescent current can be deduced. A large number of solutions was proposed over the years with the aim to obtain a power consumption reduction without impacting negatively on the accuracy of the converter, some of these involves high energy-efficient OPA, because it is the block most starved of energy. Usually the opamp works in class-A, that is the best solution for the linearity, but it also means that the power consumption is constant over time and the energy efficiency is upper limited to $\frac{1}{4}$. An higher energy-efficient OPA is the class-AB opamp, in fact in this particular class of amplifier the power consumption is related to the input signal, and the maximum efficiency is $\eta = \frac{\pi}{4}$. This solution allows high-speed conversion with low power consumption, this is possible thanks to the low static power consumption, high-speed transition and high driving capability provided by the clas-AB opamps. A possible way that allows a dramatic reduction of the power consumption is the complete replacement of the opamp with an high energy-efficient circuit based on Zero Crossing (ZCB) that performs the same function of the opamp. The latter solution saves a large part of the power consumption in the ADC because the ZCB is basically a charge pump controlled by a comparator, thus the quiescent current is very low respect to the quiescent current of an opamp. Many other solutions proposed for increase the energy efficiency act at architectural level, indeed taking into account that the operational amplifier is required only in one of the two operative phases, is possible use a reduced number of amplifier by sharing one of them every two stages with a reduction of power consumption and die area.

Chapter 2

Power consumption reduction in submicron CMOS process

The global semiconductor market will have an increase of 6.7% in 2015 to 2025 decade [9]. While the overall growth of semiconductor maret will be lower than in the past, several areeas will have substantial increase than the overall semiconductor market. One of this high growth segment is the IoT (Internet of Things), that consists of many segments, including consumer, automotive, medical, logistics and home. The semiconductor and sensor markets for IoT are projected to have a growth of 15.3%. A keyrole in IoT is played by microcontroller, wireless connectivity and nonvolatile memory. A extremely critical requirement in IoT semiconductor market is ultra-low power (ULP), which can require specialty technology process such as SOI to make high efficiency cirtuits required by mobile devices. Smartphones represent another high-expanding segment of semiconductors market. The 5G smartphones will support peak of download rate up to 1 Gbps, thus there will be need for very high speed processing and very low power consumption. The semiconductor products for the 5G applications need very high performance and very low power consumption, wich can be supported by ultra short channel technology nodes (10/7nm). The main effect of the technology scaling is an increase of the digital performance of CMOS process, an increase of the integration level on silicon die, as stated by the Moore's law. Unfortunally the same cannot be said for analog devices, in fact only the transition frequency f_t increases with technology scaling, but other important parameters such as transconductance g_m, output resistance r_0, noise, matching between the devices and signal swing are degraded. The current approach in integrated circuits market is to integrate both analog and digital circuits on the same die, anyway, many fundamental building blocks, that realize the interface between the analog and digital world can not be considered neither analog nor digital. These interface circuits are called mixed-signal integrated circuits (MS-IC), and in MS-IC design different problem as the intereferences to the analog side are

generated by the switching activities of the digital circuit. The MS-ICs are highly attractive for the electronics market because they have the potential of reducing space occupation and power consumption, by substituting many discrete devices, eliminating inter-chip board connections, and increasing hardware reliability. The large amount of digital processing power, at essentially low energy cost, allowed by deep submicrometer technologies, enables the implementation of techniques which relax the specifications of analog circuits by compensating analog imperfections with digital algorithms. This idea leads to digitally assisted analog circuits, and one of the most important techniques in this field is digital calibration of analog-to-digital converters. A large part of the market of electronics devices is implemented in CMOS technology, recently, for RF applications also BiCMOS technology has been used. These processes also have bipolar devices, but are more expensive than standard CMOS, because they need for more processing steps during the manufacturing, and when possible the preferred choice is to implement all the analog, mixed-signal and RF in standard CMOS technology. The choice of thecnology node is driven by digital applications, such as DSP, memories and microprocessors. In these applications only N-channel and P-channel MOS are required, but for analog, mixed signal and RF applications also the availability of good-quality passive device such ad capacitors, inductors and resistors is important, however the integration of these additional devices comes at the price of more processing steps and higher manufacturing costs. In the first part of this chapter will be discussed the side effects related to the deep submicron CMOS processes, and their consequences on the Analog design. In the second part of this chapter will be introduced the most common techniques for the power consumption reduction, that some of these will be applied to make a low-power ADC pipeline described in the chapter 4.

2.1 Deep Submicron CMOS Process

The ideal MOS is a four terminal non-linear active device, generally available in two versions: NMOS and PMOS. We will suppose that the physics and the behaviour of longchannel (ideal) MOS devices is known, in order to focus on short-channel effects. For an indepth analysis of MOS devices, see [10]. In most processes, both NMOS and PMOS devices are available, generally of the enhancement type: depletion devices aren't generally available. In advanced processes, several NMOS and PMOS devices may be available, optimized for high-voltage, low-leakage and/or high-speed performance, and also different threshold voltage are available.

2.1.1 Static Charateristic of NMOS Devices

If we neglect body and channel length modulation effects, the NMOS has three regions of operations, depending on the gate-to-source V_{GS} and the drain-to-source V_{GS} voltages, as it is described by these static equations:

$$I_G = 0$$
$$I_D = -I_S = \begin{cases} \beta(V_{GS} - V_{TH})^2 & \text{if } V_{GS} > V_{TH} \text{ and } V_{DS} > V_{GS} - V_{TH} \\ \beta(2(V_{GS} - V_{TH}) - V_{DS})V_{DS} & \text{if } V_{GS} > V_{TH} \text{ and } V_{DS} < V_{GS} - V_{TH} \\ 0 & \text{if } V_{GS} > V_{TH} \end{cases} \tag{2.1}$$

V_{TH} is the threshold voltage, $\beta = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}$ is the non-linear transconductance, μ_n is the electron mobility, $C_{OX} = \frac{\epsilon_{OX}}{t_{OX}}$ is the specific capacitance of the channel, while W is its width and L is its length, ϵ_{OX} is the absolute permittivity of silicon dioxide and t_{OX} is the gate oxide thickness.

2.1.2 Small Signal Properties of NMOS Devices

The ideal NMOS device, in saturation, has the following small-signal model and parameters:

$$\begin{cases} i_G = sC_{GS}v_{GS} \\ i_D = g_m v_{GS} \\ i_S = -(g_m + C_{GS})v_{GS} \end{cases} \tag{2.2}$$

Where:

$$\begin{cases} C_{GS} & = \frac{2}{3}C_{OX}\frac{W}{L} \\ g_m & = 2\beta(V_{GS} - V_{TH}) \end{cases} \tag{2.3}$$

In the triode region, instead:

$$\begin{cases} i_g &= sC_{GS}v_{GS} + sC_{DS}v_{DS} \\ i_d &= g_m v_{GS} + (g_o - sC_{DS})v_{DS} \\ i_s &= (g_m - sC_{GS})v_{GS} - g_o v_{DS} \end{cases} \tag{2.4}$$

Where

$$\begin{cases} C_{GS} &= C_{DS} = \frac{1}{2}C_{OX}\frac{W}{L} \\ g_o &= 2\beta(V_{GS} - V_{TH} - V_{DS}) \\ g_m &= 2\beta\|_{DS} \end{cases} \tag{2.5}$$

2.1.3 Noise Properties

Noise in the ideal MOS device is all due to thermal noise in the channel, because of collisions between charge carriers and the lattice. Thus, noise is Gaussian and white, and can be modelled as a current between the drain and the source terminals of the device. For a NMOS in saturation, the noise power density is given by:

$$S_n(f) = \frac{8}{3}K_B T g_m \tag{2.6}$$

In the triode region, for $V_{DS} = 0$

$$S_n(f) = 4K_B T g_o \tag{2.7}$$

These are the two regions of operation in which we are interested in the following, as operational amplifiers work in saturation, and switches work in triode region with $V_{DS} = 0$.

2.1.4 Short Channel Effect

The model which describes the ideal behaviour of a MOS device does not describe accurately a device manufactured in deep submicron technology node. The well know channel length modulation, and also the body effect bring a large number of undesired effects on the MOS behaviour, which impact on DC-gain, noise and leakage current. A MOS device is considered to be short when the channel length is the same order of magnitude as the depletion-layer widths (x_{dD},x_{dS}) of the source and drain junction. As the channel length L is reduced to increase both the operation speed and the number of components per chip, the so-called short-channel effects arise.

2.1.4.1 Output Resistance

In a ideal MOS transistor in saturation region the drain current is independent on V_{DS}. Here hence the DC-gain of a common source configuration should be infinite,

but obviously with real devices the DC-gain is finite. The dependence of the drain current I_D with the drain to source voltage V_{DS} it is due to the channel-length modulation effect, which consists in the modulation of the length of the channel due to the widening of the pinch-off region with V_{DS}. For high values of V_{DS}, the channel transports more current, as if the channel length of the MOS device were shorter. In short-channel devices there are two effects which reduce output resistance [11]: drain induced barrier lowering (DIBL) and substrate current induced body effect (SCBE). DIBL is a modulation of the threshold voltage dependent on the drain voltage, while SCBE is a substrate current induced by the formation of hot carriers due to the high electric field in the channel. This substrate current flows from the drain to the substrate and does not involve the source, and it results as a reduction of the resistance value seen by the drain. There are complicated expressions which describe the dependence of these effects on device geometries and doping levels, as can be seen in [11], but in a first order approximation all these effects can be bundled together in a single Early voltage parameter λ

$$I_D = K(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{2.8}$$

2.1.5 Body Effect

The threshold voltage of the MOS transistor can be modified through the polarization of the fourth terminal of the device, more precisely by the polarization of the body to source junction as described by

$$V_{TH} = V_{T0} + \gamma \left(\sqrt{\Phi_F - V_{BS}} - \sqrt{\Phi_F} \right) \tag{2.9}$$

where:

$$\Phi_F = \frac{K_B T}{q} ln \left(\frac{N_A}{n_i} \right) \tag{2.10}$$

and

$$\gamma = \frac{\sqrt{2q\epsilon_{Si}N_A}}{C_{OX}} \tag{2.11}$$

and where N_A is the channel p-doping level, n_i the intrinsic carrier concentration of silicon, q the unit charge and ϵ_{Si} the permittivity of silicon. When the body voltage increases the threshold voltage decreases due to the body effect, and the drain current increases. Thus the body acts as the second gate of the device, but the body to drain transconductance g_{mb} is lower than gate to drain transconductance g_m, and also the input impedance of the body terminal is not purely capacitive.

2.1.6 Modification of the Threshold Voltage due to Short Channel Effect

The equation giving the threshold voltage at zero-bias

$$V_{TH} = V_{FB} + 2\phi_F + \frac{\sqrt{2\epsilon_S q N_a (2\phi_F + V_{SB})}}{C_{OX}} \tag{2.12}$$

is accurate in describing large MOS transistors, but it collapses when applied to small-geometry MOS. In fact that equation assumes that the bulk depletion charge is only due to the electric field created by the gate voltage, while the depletion charge near n^+ source and drain region is actually induced by pn junction band bending. Therefore, the amount of bulk charge the gate voltage supports is overestimated, leading to a larger V_{TH} than the actual value. The electric flux lines generated by the charge on the MOS capacitor gate electrode terminate on the induced mobile carriers in the depletion region just under the gate. For short-channel MOS, on the other hand, some of the field lines originating from the source and the drain electrodes terminate on charges in the channel region. Thus, less gate voltage is required to cause inversion. This implies that the fraction of the bulk deplition charge originating from the pn junction depletion and hence requiring no gate voltage, must be subtracted from the V_{TH} expression. The shift of the threshold voltage is proportional to the ratio x_j/L (where x_j is the junction depth), and becomes more prominent in short channel MOS, and approaches zero for long-channel lenght MOS where $L >> x_j$

2.1.7 Parasitic Capacitances

Dynamic models of real MOS devices do not only have the channel intrinsic capacitance, but also extrinsic parasitic capacitances. The main extrinsic parasitic capacitances are $C_{GD,ol}$, $C_{GS,ol}$, $C_{BD,j}$ and $C_{BS,j}$, where the two capital letters show the terminals between which they are connected. Overlap capacitances, dubbed 'ol', are due to fringe effects between the gate and the silicon, while junction capacitances, dubbed 'j', are mainly due to the parasitic inverse-biased diode between the n^+ wells and the p substrate.

2.1.8 Mobility Degradation and Velocity Saturation

The standard equation of the ideal MOS are derived under two assumption: the first one is that carrier velocity is proportional to the horizontal electric field, and the second assumprion is that carrier mobility is independent on the vertical electric field. Starting from these two assumptions, the classic square-law of the current in MOS devices can be obtained. However, for high values of horizontal electric field between the drain and the source, the velocity of the carriers saturates to an

asymptotical value. The relation between horizontal electric field E_h and carrier velocity v_n can be written as

$$v_n = \frac{\mu_n E_h}{1 + \frac{E_h}{E_c}} \tag{2.13}$$

where E_c is the critical value dependent on the technology. For low value of horizontal electric field the linear approximation can be used, but for higher horizontal electric field values the velocity tends to saturate and to remain constant. In a short channel device, where the vertical dimension is comparable with the horizontal, the vertical field has an impact on mobility, because a large vertical field "compresses" the channel nearer to the oxide. At the interface between the channel and the oxide, mobility is lower than in the bulk of the lattice, these surface effects are due to lattice imperfections at the interface between silicon and silicon dioxide. The mobility of the carrier can be modeled as function of the vertical field between the gate and the channel, which depends on $V_{GS} - V_{TH}$

$$\mu_{n,eff} = \frac{\mu_n}{1 - \Theta(V_{GS} - V_{TH})} \tag{2.14}$$

These effects cause the drain current to be no longer quadratically dependent on V_{GS}. In short-channel devices, where electric fields reach high values because dimensions shrink more than voltage levels, and where doping levels are higher, this causes the drain current to be linearly dependent on V_{GS}, thus the transconductance g_m that is the derivative on V_{GS} of I_D will be constant with V_{GS}. A standard model which is often used to take into account this effect is called the Hodges model, in which the saturation current is given by

$$I_D = \frac{K(V_{GS} - V_{TH})^2}{1 + \eta(V_{GS} - V_{TH})} \tag{2.15}$$

2.1.9 Leakage Currents

In the ideal MOS for V_{GS} below the threshold voltage no current should flow, and also for V_{GS} above V_{TH} no static current on gate or body should flow in every operating condition. However, in short-channel devices substrate and gate current, and also sub-threshold drain current are shown. These currents are due to several non-ideal effects which were negligible in long-channel devices, but must be taken in account in deep submicrometer technologies. Drain current in sub-threshold operation is due to carriers present in the substrate when the channel is not present, because $V_{GS} < V_{TH}$. This is a diffusion current, and it depends exponentially on the external voltages like in bipolar devices, and can be described as

$$I_D = I_t \frac{W}{L} exp\left(\frac{V_{GS} - V_{TH}}{nV_{TH}}\right)\left(1 - exp\left(-\frac{V_{DS}}{V_{TH}}\right)\right) \tag{2.16}$$

Where n is a parameter related to the body effect. The dependency on V_{DS} can be neglected for $V_{DS} > 3V_{TH}$.

High level of electrical field causes the substrate current, because this high electrical field creates hot carriers which, impacting against the crystal lattice, create electron-hole pairs which flow from the drain to the body. This current depends on V_{DS}:

$$I_{DB} = K_1 I_D (V_{DS-V_{OV}}) exp\left(-\frac{K_2}{V_{DS} - V_{OV}}\right) \tag{2.17}$$

Gate current can be present because of tunnelling of the oxide, which can occur for thin oxide layers and high gate-to-source voltages. Tunnelling occurs because of tunnel effect or because of hot-carrier effects. In the former case, it is a quantum mechanical effect; in the latter case, high-kinetic energy carriers pass beyond the potential barrier and flow toward the channel.

2.1.10 Noise

In submicrometer channel lenght devices, a high level of flicker noise and an excess of thermal noise are shown. Moreover, for high frequency also gate noise occurs due to the capacitive coupling between gate and channel. This noise is called "pink noise", and it is relevant in RF applications. Flicker noise, also called $1/f$ noise, is present in all active and passive devices, and the most part of its power spectral density is concentrated at low frequency. For high frequencies the flicker noise in completely submerged by the white thermal noise floor, and the frequency at which the two power densities are equal is called noise corner frequency. Its power density increases with the scaling down of transistor sizing, and, hence, small MOS devices tend to show noise corner frequency up to several MHz. Excess white noise is caused by hot carriers and other small-dimension effects, and it is modelled as noise in the ideal MOS, but with a multiplicative factor $\eta > 1$

$$S_n(f) = \frac{8\eta K_B T g_m}{3} \tag{2.18}$$

Pink noise, is due to channel thermal noise coupled to the gate by the channel capacitance. This noise can only be seen at high frequency and is correlated with white channel noise because they share the same physical source.

2.2 Inpact on Analog Design

The technology scaling brings a continuous improvement in digital applications because it allows higher performance and more integration. Sadly the characteristics of short-channel MOS devices have a negative impact on analog design, indeed the effects of scaling on MOS performance tend to make analog design more difficult.

This is due to many factors, such as low intrinsic gain, low voltage headroom, leakage currents and high noise. In addition, as well as in mature technology nodes, still the problems related to accuracy due to statistical variations of device properties (process variations). Furthermore mismatch effects are ever more tangible with the technology scaling.

2.2.1 Intrinsic Device Gain

Most of baseband circuits are based on feedback loops, in which the closed loop accuracy is higher as the open loop gain is higher. High gain makes more effective the feedback in terms of desensitisation to process variations, minimizing the error function, and reducing the distortions. Unfortunately, short-channel devices tend to exhibit very poor intrinsic gain, as a matter of fact, in saturation region the output conductance is no more than 10-20 times smaller than the transconductance. Thus, the gain of a MOS transistor would be limited to 10-20 (20-26dB). Consequently, in order to obtain the high gain needed (80-100dB) to reach high accuracy, multi-stage operational amplifier are required. Multi-stage structure means high power dissipation and low bandwidth due to compensation nets. Must be noted that 80-100dB is the gain of a NPN transistor. Taking as example: a standard common-source amplifier with active load, employing NMOS and PMOS devices implemented in 350nm technology has a gain of about 30dB, while in 130nm the gain of the stage may fall below 20dB. Fortunately enough, intrinsic gains below 20dB would cause problems also in digital applications, because the transition region of CMOS inverters would be too wide. As digital applications are the main driver of the electronics market, it may be expected that technologist will be asked to avoid this dramatic reduction of per-stage gain.

2.2.2 Signal Headroom

The voltage supply in short channel technology nodes is scaled down, because when the size of the devices are reduced, if the voltage supply is not scaled down the electrical field will increase and bring relaiability issue due to breakdown. The reduction of the voltage supply improves the energy efficiency of digital circuits, but sets a limitation on the dynamic range of analog circuits. Sadly, for reasons related to the leakage current, the threshold voltage can not be reduced linearly with the power supply voltage, thus stacked structure whith more than 4 MOS devices can not be taken in account in these technologies.

2.2.3 Excess Thermal Noise

The dynamic range of the analog circuit implemented in deep submicron CMOS process is also limited by the excess thermal noise. Indeed, in these technology nodes

the noise floor can be from 2 to 6 time higher than the prediction of the model. This is the same to a reduction of the noise performance for a defined quantity of transconductance. The Friis formula 2.19 say that for low gain stages, the total noise figure is more dependent on subsequent stages, and do not set by the first stage as the case of high gain stages.

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \cdots G_{n-1}} \tag{2.19}$$

where F_i and G_i are respectively the noise factor and the available power gain of the i-th stage.

2.2.3.1 Leakage currents

The leakage current is the most relevant factor of power consumption for digital circuits, where millions of CMOS logic gates consume statically tens of nano Ampere, and all together cause a huge power dissipation, also when no operations are performed. In analog circuits, this problem is less relevant because typically a lower number of MOS is employed, and most of them are used in saturation region, thus they are biased to dissipate statically. However, in a very important circuital technique namely switched-capacitor the leakage current has a severe impact on the performance. In fact, in circuits, which comprise sample and hold, ADC and discrete-time filters, the signal is stored on capacitors, and the leakage current damage the stored information because the capacitors lose their charge.

2.2.4 Mismatch and Process Spreads

One of the main advantages of digital design with respect to the analog design is the desensitization to the process spreads and mismatch ([12], [13], [14]). Process spread is defined as variations of device properties between different dies and different wafers. When a chip is produced, it will be fabricated on thousands of wafers and hundred of thousands of different dies. The process spreads cause the variation in the threshold voltage of the MOS devices, on the resistance of polysilicon strips, and a distribution on the unit capacitance of capacitors. The process variation distribution is generally Gaussian with the mean on the desired value, and a variation of $5 - 20\%$. For a mass production of an IC process variations together with temperature and voltage supply variations must be taken into account during the design phase, because the robustness against the process, voltage supply and temperature (PVT) variations is one of the most critical specifications for a reliable integrated circuit design. Intra-chip variations between devices that should be identical cause offset voltage, as the case of the differential pair that is designed to be perfectly symmetrical. Moreover, a couple of resistors used as voltage divider may show a certain error in the voltage levels because the resistors will not be exactly identical. Mismatch can be caused

by global factors such as gradients in the doping profiles. This source of "global" mismatch, can be caused by a not perfect alignment of process machinery and wafers during the manufacturing process. However, the dominant mismatch effect in short-channel active devices is not due to gradients and other global mismatch sources, but it is due to local variations. In this case, each device's channel having a certain number of doping ions, whose number can be in the order of 100 in advanced CMOS processes, local mismatch can arise because this number can vary among nearby devices.

2.3 Analog Design in Mixed-Signal Systems

In a mixed-signal system both analog and digital circuits coexist. While digital circuits are robust against the interference caused by the analog circuits, the same can not be said for the analog part, which suffers for the presence of digital circuits that cause interference which degrades the performance of analog block. These disturbances can have different causes such as power supply coupling, substrate coupling, and inter-wire crosstalk.

2.3.1 Switch

In the previous chapter when switched-capacitor techniques were described all switches were considered to be ideal. The simplest switch structure is the pass transistor, and can be made both with a P-cannel or an N-channel MOS device. In an ideal case the switch's on-resistance is zero, but in the real case the resistance can not be equal to zero. However the on-resistance must be as lower as possible not to limit the charge of the load capacitor. The main issue for the pass transistor is the dependence of the switch's resistance with the gate-to-source voltage, and thus with the input signal. The worst case for an N-channel pass transistor in when the input signal is high, and thus the gate-to-source voltage is near the threshold voltage, in this case the resistance of the switch is maximum. Conversely the dual case occur for the P-channel pass transistor when the input signal is low. As a result both the P-channel and N-channel pass transistor are unsuitable in all those applications where high dynamic signal is required.

The transmission gate (figure 2.1) makes use of both PMOS and NMOS devices to improves the dynamic range of the switch. With transmission gate is possible attain a reduction of the switch on-resistance in both the marginal upper and lower regions. As a result the on-impedence is very low for a wide region, thus transmission gate is suitable for applications where high dynamic swing of the signal is required. With the technology scaling the voltage supply was redced to overcome breakdown due to extremely high electric field, but the threshold voltage was mantained at high level to reduce the leakage currents. This has caused some issues on the switch

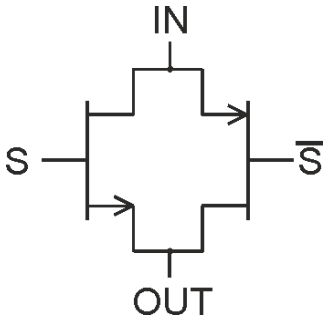

Figure 2.1. Transmission Gate

performance, the main one is the lower conductance when the supply voltage is lower than $2V_{TH}$, in fact the conductance could go to zero, because both the transistor would be off.

$$\begin{aligned} G_{SW} &= G_N + G_P = 2\beta_N(V_{DD} - V_{IN} - V_{TH_N}) + 2\beta_P(V_{IN} - V_{IN}V_{TH_P}) \\ &= 2\beta_N V_{DD} - 2\beta_P V_{TH_P} - 2\beta_N V_{TH_N} + (2\beta_P - 2\beta_N)V_{IN} \end{aligned} \tag{2.20}$$

The last equation is valid for $V_{IN} > V_{TH_P}$ and $V_{IN} < V_{DD} - V_{TH_N}$. Beyond $V_{DD} - V_{TH_N}$, only the channel-P transistor is on, and the transconductance of the switch is $G_{SW} = G_P = 2\beta_P(V_{IN} - V_{TH_P})$; conversely before V_{TH_P}, instead, only the channel-N transistor is on, and the total transcondictance is equal to $G_{SW} = G_N = 2\beta_N(V_{DD} - V_{IN} - V_{TH_N})$. If the transconductance of the two transistors is the same, in the central range the switch impedance is independent on the input level.

In order to overcome this limitation in low-voltage applications, a voltage doubler can be used. An NMOS switch with clock voltage doubler is shown in figure 2.2. The voltage applied at the gate of the pass transistor switches between ground and $2V_{DD}$. This structure might suffer of reliability issue due to breakdown limitations if $2V_{DD}$ is higher than the maximum gate voltage of the devices.

Another enhancement of the performance of switches is given by input-dependent bootstrap shown in figure 2.3. In this kind of switches the gate-to-source voltage is kept constant, because, when the switch is on, a voltage equal to the input voltage plus the supply voltahe is forced on the gate of the switch. This expedient maximizes the linearity, because the conductance of the switch is almost independent on the input signal. Also this implementation can suffer for reliability problems due to the high voltage value in the circuit.

2.3.2 Supply Noise

One possible path of communication between analog and digital circuits is the power supply node. Most of digital circuits, first of all static CMOS logic family, consume a variable quantity of current from the power supplies. The power consumption for

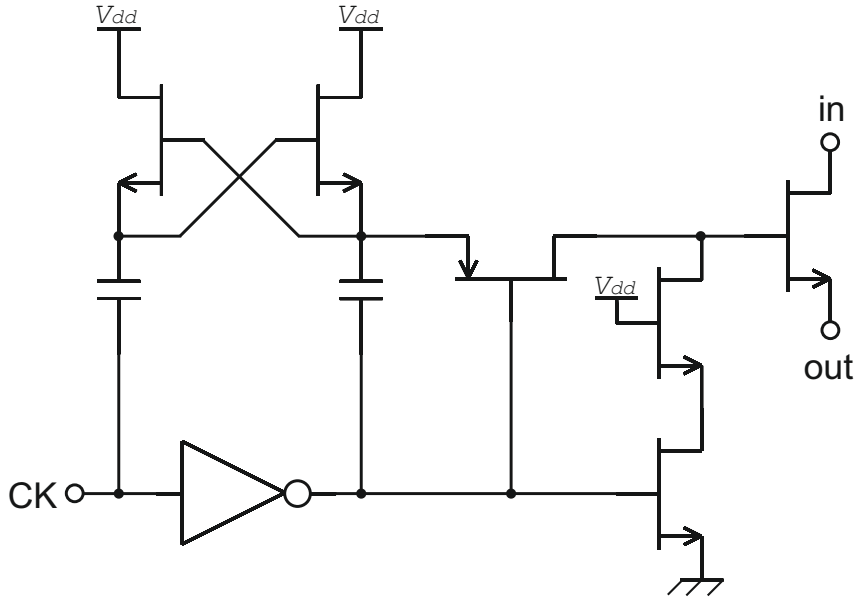

Figure 2.2. NMOS switch with clock voltage doubler

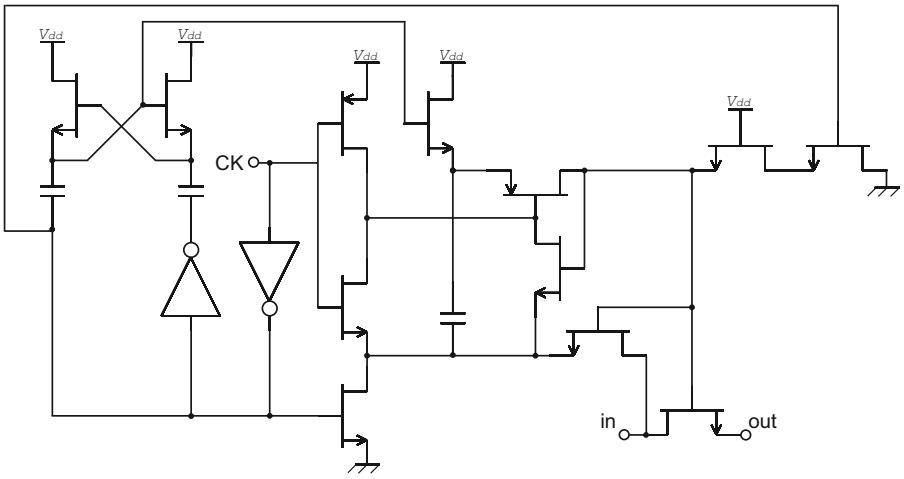

Figure 2.3. Signal dependent bootstrap

digital circuits realized whith static CMOS gates can be identified in three parts, first of all the dynamic current due to the charging and discharging of the gate capacitors, the second component is due to short-circuit current that flows between the power supply and ground during the switching activity of the logic gate, and the third component is due to the static current due to the leakage. Thus, considering the figure 2.4 where the T-type LC tank models the pad and the wire bond that

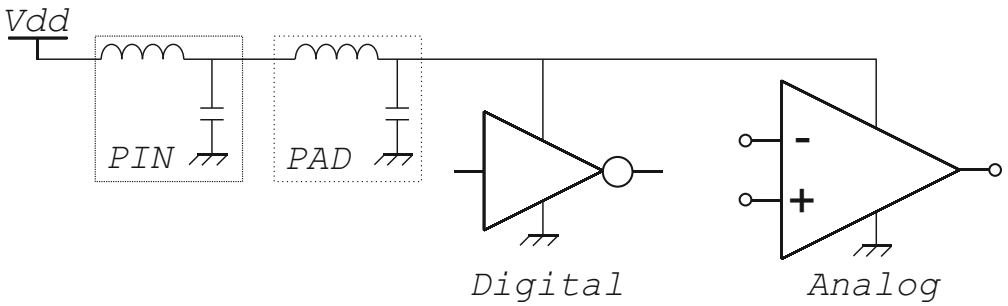

Figure 2.4. Baseline Mixed-Signal integrated Circuit

connects the circuit to the external voltage source. When the digital circuit toggles, the load and parasitic capacitances has been charged or discharged. This causes a variation on the current that flows through the pin and pad, and thus also the voltage applied on the analog circuit is influenced, because the LC circuits that connects the ideal supply and the circuits. In this way, the behaviour of the analog circuit will be modified by the switching of the digital circuit, and this is a likely cause of distortions. Dynamic power consumption is the most important source of power supply noise, because the power supply and the circuit are connected by an inductive load. However, a resistive component would cause the power supply to be dependent even on static leakage variations, which would modify the voltage drop on the resistor, and, hence, the supply voltage of the analog circuit. This form of interaction is called inductive noise.

2.4 Power Consumption Reduction Techniques

Pipelined ADCs provide higher resolution with lower power dissipation compared to flash ADCs. Pipelined ADCs can operate at higher speeds compared to SAR ADCs since multiple samples of the input are processed simultaneously in multiple stages of the pipeline. Hence, pipelined ADC provides higher resolution with lower trade-offs in power and speed among the Nyquist rate ADCs. Applications such as high definition displays and wireless LAN require high performance analog to digital converters operating at medium to high speed, for these applications, the pipelined ADCs are preferred. For applications such as portable wireless devices, power dissipated by pipelined ADC needs to be reduced. For this reason, the research on this topic has

lead to different solutions to achieve a reduction of the power consumption. Some solutions can be used regardless the specific architecture of the ADC, while other solution can be applied only on specific ADC structures. Sure enough in all the ADC structures the great part of the power consumption is due to the operational amplifiers used. Therefore the optimization of the opamp allows to achieve high power-efficiency ADCs. The design of a high-gain and high-speed opamp with low power consumption has been the greatest challenge in the design of ADC. The power consumption of an opamp is related to its load capacitance, bandwidth, DC-gain and slewrate. Thus, a possible way is choose of a better energetic-class for the opamp, such as class-AB instead class-A. In fact, the maximum energy efficiency of the class-AB opamp is higher than the efficiency of the class-A amplifier. Moreover, the power consumption of a class-AB amplifier is mainly due to the dynamic consumption,and the variability of the power consumption with the effective amount of charge injected or sinked to the capacitive load can be exploited to obtain a reduction of the wasted energy. In particular, in mixed signal systems where the analog signals are sampled by Sample-and-Hold is useful keep as slowest is possible the sampling rate (but sufficient to avoid aliasing), in order to limitate unnecessary charge and discharge of the sampling capacitors during the sampling phases. This led a linear reduction of the power consumption with the reduction factor of the sampling rate. This operation can be applied for all kind of ADCs, but a major effect is obtained in all those ADC structures that use a great number of opamps as the flash or pipelined converters. Another expedient that can be used to attain an improvement in power consumption is the reduction of the voltage supply value. This can be done using particular opamp structure, but causes a limitation in the dynamic of the signal. Moreover, with low voltage supply the stacked structure can not be used, then the voltage gain of the opamp decreases. The most simple low-voltage amplifier structure that works in class-AB is the CMOS inverter, that can work with a power supply lower than $2V_{TH}$ and allows dynamic scaling of the voltage supply and conversion frequency. Calibration also can be considered another kind of power reduction technique, in fact, it is possible to use very low-power amplifiers with low gain or open loop amplifiers, and correct all the errors in digital domain at a lower energetic price. Also it is possible to use small values for the sampling capacitors, that allows high charging speed and also high conversion speed, but capacitors of small value suffers for mismatch, and thus the conversion can be affected by error. Also in this case digital calibration tecniques can help to correct the analog eror and achieve the wished linearity for the ADC. Otherwise, can be used techniques for increasing the energy efficiency developed for a specific ADC architecture. For the pipelined ADC, in addition to the above mentioned generic techniques is possible increase the energy-efficiency applying techniques such as the opamp-sharing, or by the replacement of the opamp with a comparator based circuit, or also, under determined condition, by removing the front-end sapmle and hold. This chapter

continues with the description of the cited techniques.

2.4.1 Frequency Scaling

The power consumption of a circuit can be divided in static and dinamic power consumption. The satic power consumption is constant in time and has not dependence with the signal, it is due to the quiescent current of the circuit. The dynamic consumption is variable in time and is related to the signal. In SC circuits, where the circuit is reconfigured during the different phases, the dynamic consumption is also related to the clock signal. Thus, in SC circuits, the dynamic power consumption has a linear relation with the frequency of the clock signal. This linear relation can be exploited to obtain a reduction of the power consumption through a limitation of the conversion speed. Obviously the conversion speed must respect the Nyquist relation with the signal bandwidth to overcome aliasing effect.

2.4.2 Voltage Scaling

In digital circuits scaling the voltage supply allows an improvement of the energy efficiency due to the reduced switching power [15], this can be done when the speed requirement is relaxed. Generally, this technique can not be applied to analog circuits, because the power consumption is usually dominated by static power required for thermal noise constraints, but in some ADCs where the digital part is dominant, such as SAR ADC [16], [17], flash ADC [18], [19] and ringVCO based sigma-deltaADC [20], good energy efficiency can be reached at low voltage supply, because the power consumption in this ADCs is dominated by the switching power. Anyway the reduction of the voltage supply is payed with the reduction of the voltage swing of the signal, that is also related with the SNR, thus the minimum voltage supply can be limited by the termal noise. Furthermore the voltage supply is related with the maximum conversion frequency wich can be used unless incomplete settling effect degrade the ENOB of the converter. In some cases can be applied a dynamic voltage scaling on both digital and analog circuits of the ADC. This can be done only when the speed requirements are reduced to overcome incomplete settling of the signal. The dynamic voltage scaling brings a significant reduction of the power consumption, but places limitations on the circuit structures.

2.4.3 Open Loop Amplifier Approach

Usually an opamp is closed in a feedback loop because the reaction improves the linearity and allows to set the gain on a precise value. The main side effect of the feedback is due to the reduction of the bandwidth for a factor equal to the reaction ratio. As a result pipeline stages with large closed-loop gains come at the cost of lower maximum speed. To overcome this limitation, open-loop amplifiers can be

used to obtain higher speed with the same power consumption, or reduce the power consumption for a given speed. A significative advantage of an open-loop topology is found in the simple operational amplifier structure that can be used. In fact, a simple differential pair can be used as open-loop amplifier. The main advantage of the open-loop approach is that the stability of the opamp does not represent a constraint. Furthermore, with an open-loop amplifier, high DC-gain and bandwidth can be obtained using simple circuital structure it would be easier to operate with low supply voltages. The drawbacks using an open-loop topology approach is that the linearization and process desensitization due to the feedback are eliminated. In fact, in closed-loop circuits the large open-loop gain of the operational amplifier creates a virtual ground at the input of the opamp and thus significantly reduces the input signal swing to the input differential pair of an opamp, resulting in a very linear closed-loop transfer curve. In open-loop circuits the input swing has the value of the output swing divided by the DC-gain. As a result, the transfer curve of an open-loop approach suffers from a significantly increased non-linearity. Furthermore, in a feedback circuit, the gain is set by the ratio between the capacitors, that can be set with high accuracy, whereas in open loop circuit the gain is set by the product of the transconductance g_m and the load resistance R_{load}, that can vary significantly with process and temperature. To overcome nonlinearities and gain variation a calibration technique is required in open-loop systems. The calibration technique which corrects in digital domain the nonlinearity uses an inverse nonlinear function $f^{-1}(x)$ and statistic based digital background technique is used to estimate the value of $f^{-1}(x)$. The specific details of this calibration scheme are not discussed here, however, it should be noted that calibration engine is mathematically intensive due to a large number of calculations needed for digital estimation of $f^{-1}(x)$. Thus as the bandwidth is dramatically increased in an open-loop circuit for a given power, also the power of the digital calibration would be increased to enable the bandwidth enhancement. However, the process scaling favours the digital circuit in term of area and power consumption respect the analog ones. Hence the open-loop approach is a promising trade off between analog power and digital complexity for nanometric channel length technologies.

2.4.4 Specific Power Reduction Techniques for Pipelined ADC

In the previous section generic techniques developed to achieve reduction of power consumption in ADC that can be applied regardless to the architecture are reported. Some other techniques are developed to reduce the power consumption of specific ADCs structure. In this section are reported the techniques that can be applied only in pipelined ADC.

2.4.4.1 Front-End Sample-and-Hold Removal

Usually,in ADC pipeline, a front-end Sample-and-Hold circuit is used to ensure that the MDAC and subADC process the same input. This increases the power consumption. To reduce the power consumption, several techniques that allow a pipeline ADC to operate without the front-end Sample-and-Hold are available. As reported in [21] - [22] the front-end Sample-and-Hold can be eliminated introducing a redundancy of the first stage. For a 1.5-bit MDAC architecture, the offset of the sub-ADC can be as large as $V_{ref}/4$. Therefore until the difference between the input of the MDAC and subADC is less than $V_{ref}/4$, the effect of sampling skew appears as an input-referred offset on the subADC comparator, and the effect of the offset can be eliminated by the redundancy of the first stage. Hence the front-end Sample-and-Hold can be eliminated without any further modification to the ADC. Assuming a sinusoidal input to the ADC with a full scale voltage aplitude, and assuming no inherent offset in the subADC comparators, the maximum allowable skew time that can be corrected by the redundancy of a 1.5 bit stage is $(8\pi f_{in})^{-1}$. However for a precise calculus of the maximum allowable skew, also the mismatch of the comparators in the subADC must be taken in account because it can be large.

2.4.4.2 Capacitors and Opamp Sharing

A significant source of power dissipation is represented by the opamps inside the MDAC blocks, they have to be designed to satisfy the gain and bandwidth constraints of the MDAC and for this reason they result the most power hungry block in the whole pipelined ADC. A large number of techniques have been reported in the literature with the aim to obtain a reduction of the power consumption. In [23] the switched-opamp technique is proposed, here the opamp is turned off during the sampling phase because it is not used (this statement is true until no correlated double sampling technique is adopted to cancel the offset of the opamp), but the maximum conversion speed of the ADC is limited to the turn-on delay of the opamps. Opamp sharing and capacitor sharing are efficient techniques that can be applied in a pipelined ADC to achieve low power operation. In simple pipeline structure, the amplifier is used only during the error's amplification phase but not during the sampling phase, thus in the pipeline chain where the stages are alternatively in sampling phase and in error amplification phase, only half of the opamps are effectively required. In opamp sharing techniques one opamp is shared between two adjacent stages, because only for one of them the opamp is required. The main issue in this approach is the memory effect, that is due because the opamp is used continuously in both phases, and there is no time to reset the input. Many techniques have been reported in the literature for opamp sharing and for resolving the issues due to sharing [24],[25],[26],[27]. Split sharing technique may be adapted to alleviate this problem. In this technique, opamp is realized using two stages and

the second stage of the opamp is shared and the first stage is made separate for the two MDAC stages [28]. Eventhough the memory effect is resolved, the reduction in power consumption and area are not as large as only one stage is shared. In [26], [27] an additional cascode pair is used which acts as input device for one phase. In [24], additional set of input pairs are used for each phase.

Capacitor sharing is another approach proposed for low-power medium speed pipelined ADCs. Combined use of both capacitor and opamp sharing provides significant power reduction in pipelined ADCs [24]. In a SC-MDAC a capacitor is used to close a feedback loop which consists of two phases of operation, sampling and error amplification. During the error amplification phase the total capacitive load for the MDAC is

$$C_{L_n} = ((1-\beta)C_{f,n} + C_{s,n+1} + C_{f,n+1}) \tag{2.21}$$

where β is the feedback factor, C_{L_n} is the capacitive load and $C_{f,n}$ the feedback capacitor for the n-th stage, and $C_{s,n+1}$ and $C_{f,n+1}$ the sampling and feedback capacitors for the $n+1$-th stage. On the $C_{f,n}$ is stored the residue value which has to be fed to the next stage for sampling purpose. In capacitor sharing technique ([24], [29],[30]) the feedback capacitor in stage n functions both as the sampling capacitor and feedback capacitor for the $n+1$-th stage which reduces the effective load capacitance of the opamp to

$$CLshared, n = ((1-\beta)C_{f,n}) \tag{2.22}$$

In [24], the capacitor sharing technique has been applied between Sample-and-Hold and the 1-st MDAC. [29], capacitor sharing has been applied between MDAC1 and 2 and between MDAC 3 and 4 alongwith opamp sharing. But the opamp memory effect, degrades the performance of these ADCs. In [30], capacitor sharing has been extended to three stages but opamp sharing is not applied.

2.4.4.3 Comparator Based Switched Capacitor Circuits

Comparator Based Switched Capacitor (CBSC) circuits overcome limitations due to technology scaling by replacing the opamp of the MDAC with a more energy efficient structure. In a switched capacitor circuit the fundamental role of the opamp is to provide a virtual ground to ensure accurate charge transfer between the sampling and hold phases. In CBSC circuits the opamp is replaced by a comparator, and the virtual ground is emulated with a feedback loop.

Figure 2.5 show a CSBC circuit which provides gain of two. During the ϕ_1, the input is sampled on capacitor C_1 and C_2. The node V_x is initialized to a value below to the value V_x would be if an opamp where used. During ϕ_2, the charge pump at the output is turned on, and the node voltage V_x increases. When the node V_x reaches

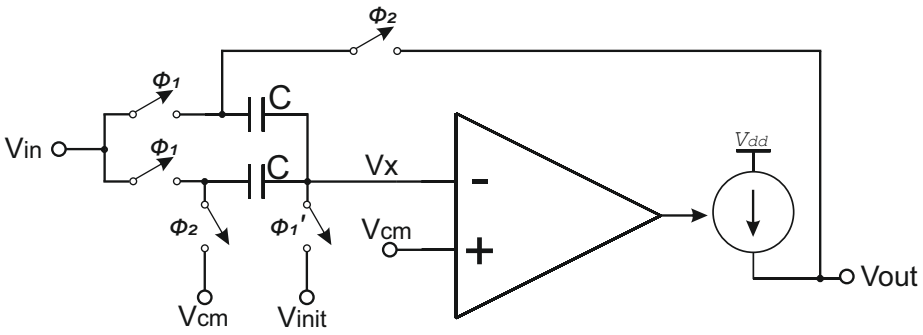

Figure 2.5. Comparator Based Switched Capacitor X2 circuit

the value V_{CM} the comparator switches off the charge pump. The voltages at the node V_x and V_{out} appear the same as if an opamp were used to create the virtual ground. The CBSC realizes the same functionality as an opamp based arrangement. The main advantage of the CBSC is that the topology does not depend on an opamp which would otherwise require a large DC gain. The comparators can be easily designed even with low supply voltages and transistor that have low intrinsic gain, this makes CBSC suitable for deep submicron technologies. Moreover [31] show that the CBSC approach is less susceptible to the thermal noise than an opamp based approach, thus smaller sampling capacitors can be used, therefore lower power consumption is required.

Chapter 3

Calibration

Mixed-signal systems are characterized for the presence of both analog and digital circuits in the same chip, and for the aforementioned motivations the analog part of the system suffers for the short channel effects related to submicrometer technologies and for the side effect due to the presence of the digital circuits on the same chip. Then seems that mixed-signal design puts only limitations on the analog performances, but this design effort is payed by a reduction of costs, weight and size of the chip. At the opposite of analog design, digital circuits performances are increased in deep submicron technology nodes, therefore the large digital computing-power allows a different possible approach that can help the design of the system. In particular, simplest analog circuits should be adopted, with relaxed performance requirement, and correct the errors in digital domanin through calibration techniques. This can be a good low-power oriented way, because the most portion of the power consumption is due to the analog part of the system thus relaxing the performance constraints brings a reduction of the required die area and power consumption, thus at parity of performances a digitally assisted analog circuit is more efficient of a pure analog circuit. In deep submicron technology nodes, digital calibration can be adopted to overcome different problems due to devices mismatch and low gain of the devices, moreover some memory effect due to incomplete settling of the signal in switched capacitor circuits can be eliminated. Digitally assisted analog circuits can be used if the cost of better analog circuits, even though their design is feasible, is higher than the cost, generally limited, of the additional digital resources required by calibration. Digital calibration techniques are used to improve the linearity of system, in this case an ADC, through a digital estimation of the errors and a subsequent cancellation of their effect by digital post-processing. Over the years different undesired effects are taken into account, as first linear errors, successively, with the improvement of the computational-power given by advanced technology nodes, and the increasing of the weight of their undesired effects also the non linear error was taken into account, and more complex calibration techniques was developed to correct this kind of errors.

Beyond linear and nonlinear errors, when some circuital techniques such as switched capacitor are involved, also errors due to memory effect can appear. They becoming more and more significant with the increasing of the resolution and conversion rate. Thus new calibration tecniques capable to extimate and correct also memory effects are required in all those applications where medium to high conversion speed and high resolutions are required. Regardless the nature of the error under calibration, different approaches can be adopted to develop a calibration method for an ADC, more precisely a calibration technique can be based on a precise error model of a specific ADC's architecture, or otherwise, it might be a blind calibration technique that is not based on a specific model. Such kind of techniques is more versatile and is suitable to identify and correct errors of different type of converter structure, but the digital correction algorithm is generally more complex compared to a model-based techniques. However, both model-based or blind calibration techniques can be divided in different groups based on the principle of operartion, in the next section a literature survey of the state-of-the-art of digital ADC calibration approaches is reported, with particular emphasis on pipeline converters.

3.1 Calibration Overview

Analog-to-data converters are needed in an increasing number of high-speed high-accuracy applications, and very often low-voltage and low-power features are required for the feasibility of portable applications. Independently of the specific ADC architecture, the performances are limited by the non-idealities of the involved analog circuits. In this non-idealities figure quantization error, thermal noise, jitter, and specific errors related to the chosen architecture such as the finite gain error or the incomplete settling, moreover also systematic contributions due to technological and process inaccuracies. The accuracy in high-speed high-accuracy ADC is actually limited by this last mentioned systematic error. Typically, the non-linear errors in switched capacitor circuits are reduced thanks to an appropriate analog design on both schematic and layout level, but this approach leads to a sub-optimal design with significative inpact on die area and power consumption. The gap between the traditional and the optimum designs becomes even more problematic with current CMOS technology trends, which have pushed down the quality of analogue-mixed signal devices (worse modelling, less accurate and noisy devices,worse matching, full compatibility with standard digital process, etc.). Actually, for resolutions equal or greater than 10 effective bits at sampling frequency higher than 50MHz, the employment of any calibration technique is not only a desirable property, but a necessity.

3.1.1 Procedure for ADC Error Calibration

All the calibration techniques operate in two separate phases to extimate and correct the errors. During the first step the error of the output code produced by the ADC respect to a reference value is measured. In the first calibration techniques analog circuits are used for the extraction of the errors, but this tecniques involve additional transistors with consequent increasing of noise, power consumption and distortion. Such techniques are overtaken by the current digital calibration techniques that overcome the previous limitations through an errors estimation in digital domain. The Evaluation phase is the second step of the calibration procedure, and in this phase the error estimated is used to evaluate the correct output code. The specific mechanism adopted to compensate the errors is strongliy linked to the estimation process, in analog solutions both the error estimation and the evaluation of the correct code are performed in analogue domain, conversely, a digital calibration solution allows different ways, indeed the correction can be performed in analog or digital domains. Regardless of the adopted analog or digital approach, the calibration techniques can be divided considering the operations mode, more precisely if the estimation phase causes an interruption of the conversion or not, this two type of calibrations are called foreground and background techniques respectively. Commonly in foreground approches the step of error estimation is done only one time just after the power is turned on [32]. Unfortunally miscalibration might happen due to temperature or power supply variations or also for the aging of components if the system works continuosly, this is the main drawback of foreground calibration methods, and is overcome by background calibration methods [33].

3.1.2 Foreground Calibration

In figure 3.1 a foreground calibration scheme is shown.

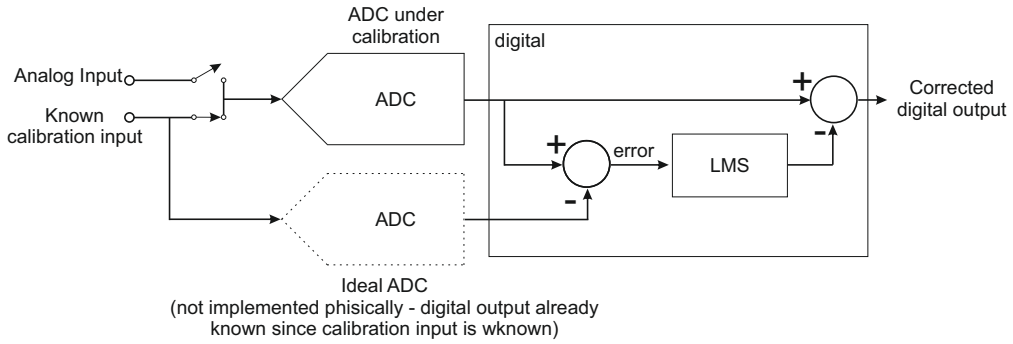

Figure 3.1. Foreground calibration principle

Foreground calibration estimates the unknown errors by interrupting normal

ADC operation and applying a known input sequence to the ADC. By comparing the output of the ADC to the expected ADC output the impact of each error source can be measured and corrected. Examples of foreground calibration in publications can be found in [34], [35]. The advantage of a foreground scheme is that calibration can be achieved within a small number of clock cycles, since the error signal labeled in figure 3.1 is highly correlated with the error sources causing the missing codes. The disadvantage of foreground calibration is that the ADC is required to be taken offline every time calibration is performed, which in some applications may not be possible.

3.1.3 Background Calibration

Background or also called online methods overcomes the limitations of foreground approach, performing the error estimation during the calibrated output computation. Background calibration continuously measures and corrects the effect of nonidealities in a pipeline stage, thus has the significant advantage that the ADC is not required to be taken offline to perform the calibration. For this reason the vast majority of calibration based publications are focused on background techniques, the large part of them use a statistics based approach to realize the calibration. In a statistical calibration scheme (Figure 3.2) the input of the pipeline under calibration is combined with a know pseudo-random sequence, thus correlating the digital output of the ADC with the pseudo random sequence can be determined the impact of the missing codes.

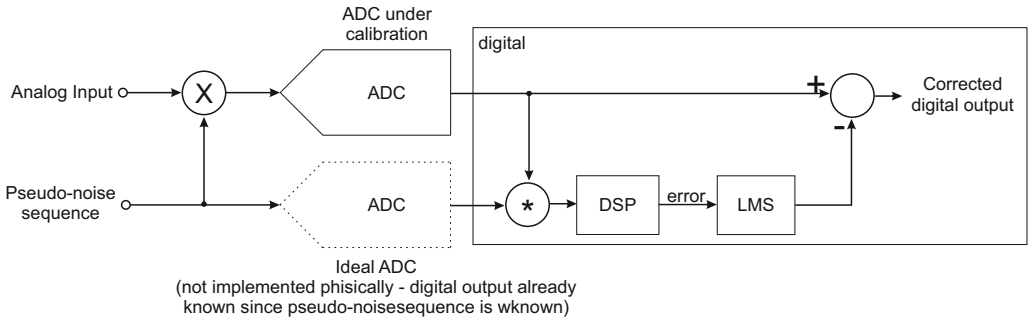

Figure 3.2. Principle of background calibration

The different background techniques can be distinguished in virtual and true background calibration approaches.

3.1.3.1 Virtual Background Calibration Technique

In virtual calibration techniques the error estimation is carried out without interrupt the conversion, but substantially still a foreground approach. The parallelism of

both estimation and correction operation can be obtained in two ways, the first one requires the use of redundant hardware [36]-[37], or otherwise creating artificial time slots for calibration purpose [38]-[39]. Redundant circuits are commonly used in order to obtain the suppression of miscalibration without break the conversion sequence. In pipelined ADC double the stage [36] or the MDAC [37] allows the quantization of the input signal while the errors are measured in background in the redundant blocks. When the circuit is calibrated, the role of the redundant hardware can be interchanged and a new calibration cycle starts. This is payed at the cost of almost doubling the die area and power consumption, furthermore, the additional switches required for the reconfiguration introduce extra noise and distortion that have an heavy negative impact on the performance and make unachievable high-performance applications. The second way to surmount miscalibration issues without interrupt the conversion sequence is to generate artificial time slots intended for the error measurement, unforunally this kind of approaches sets a limit on the bandwidth of the input signal. In [38]-[40], artificial timeslot for calibration is generated by occasionally skipping one of the input signal, which is replaced by a predefined calibration stimulus. In other solutions series [41]-[42] and parallel [39] structures make use of a queue of Sample and Hold that work at lower frequency respect to the conversion.

3.1.3.2 Skip and Fill

Another technique, called skip and fill ([43], [44]), consists in skipping the conversion of one sample to have one time slot free from the input signal which can be used to calibrate the pipeline ADC. The problem with this technique is that the missing samples would obviously cause distortions: in order to overcome this problem, interpolating polynomials are employed to predict the skipped sample. Thus, the missing sample is substituted by its prediction, and, to the extent that this prediction is correct, the skip and fill algorithm does not deteriorate the accuracy of the ADC. Interpolating polynomials are FIR filters, and they predict the missing samples by using information contained in the previous and in the successive samples: to the extent that nearby samples are correlated, interpolating polynomials can successfully predict the missing sample. White noise is an example of signal that cannot be predicted, because correlation among samples is zero, being the autocorrelation function of the white noise sequence a Dirac's delta function. The samples of a signal can be predicted if the signal's spectrum is far from being white, and the more it resembles white noise, the less it is possible to accurately predict missing samples: this technique can be used only for band-limited signals. In [45] interpolation is used to remove the effect of the input signal on the calibration procedure, without affecting the data-path.

3.1.3.3 Queue

Another way is to use a different clock frequency for the S/H and the MDAC: the effective sampling frequency of the system will be the one of the S/H, while the MDAC will work faster. This implies that there will be clock cycles in which the MDAC has no samples to convert: this spare cycles can be used for calibration. The complexity of this design lies in the need to use two separate clock frequencies (for example f_S and $\frac{11}{10}f_S$) and to interface two sampled-data systems working at different clock speeds. These techniques are called queue-based ([46], [41]).

3.1.3.4 True Background Calibration Technique

True background calibration techniques are capable to overcome the drawbacks of the virtual background approach, indeed these techniques perform a continuous measurement of the effect due to temperature and polarization variations and compensate it. Adaptive algorithms [47]-[48] can be used to generate a digital estimation of the ADC's errors. They make use of the output code of the ADC without interrupt the conversion [49]-[50]. The low impact on the analogue components, as well as the high robustness and the low power consumption of adaptive signal processing, imply significant advantages over previous background approaches.

3.1.4 Adaptive Calibration Technique

In adaptive calibration techniques some of the system parameters are amended to minimise the difference between the desired response and the actual output[47]-[48], the procedure used to select the optimal parameter values is strictly related to the chosen algorithm. The adaptive background calibration approaches can be split in two approaches: those based on channel error identification, and those called correlation-based approach.

3.1.4.1 Channel Error Identification

In channel error identification the outputs of two different paths are used to reconstruct the error function, for this purpose an aditional accurate converter with lower speed such as an algorithmic or sigma-delta architecture is involved, this auxiliary converter acts as an ideal reference for calibration [49]-[51]. In this technique the attention must be focused on the syncronisation between the ADCs. The original application for least-minimum-square algorithm was for interleaved architecture [49], but has been used for background calibration of single [49] or multi-bit [52] - [53] pipeline ADCs. Other possibility of constructing the error function in the channel error identification approach is to duplicate the entire ADC, as shown in [54]-[55].

3.1.4.2 Correlation-Based Techniques

The background calibrations based on correlation work by the injection of randomic digital sequences in the datapath. The injected sequences are not correlated with the input signal, but the method used to inject the sequences makes a correlation with the error parameters. This correlation can be exploited to exclude the effect of the input signal and all the other uncorrelated error sources and estimate the error parameters. This can be done by averaging the product of randomic signal and both the correlated and uncorrelated signal, this procedure will remove the uncorrelated terms, and in this way allows the estimation of the correlated ones, which brings with them the information related to the error. In pipeline ADC the most simple way to implement this technique is based on random swapping of the capacitors of the MDAC [56], if they are equal, as in ideal case, the swapping will not have any impact on the behaviour of the ADC, otherwise, as in actual case the capacitors are different due to mismatch, and the random swapping creates a signal proportional to the capacitor mismatch, and also correlated with the random sequences which determine the swapping. This technique can correct only capacitor mismatch errors, but in other techniques [4] the random sequence injected is used to modulate the thresholds of the comparators in 1.5 bit MDAC. In this way the random modulation generates an output data sequence that can be used to estimate errors due to capacitor mismatch, finite gain error, input parasitic capacitance, reference voltage errors. This technique based on the injection of randomic sequence is very interesting because it does not involve the analog design, but only requires for a small modifications of the digital circuits of the MDAC under calibration. Other techniques split the capacitors in smaller pieces, and swap the capacitors randomly [57], [58], [59], [60]. While this process increases the number of error terms to be estimated, thus increasing the estimation time, they represents a suitable method to inject the random sequence. There are many variations on the theme, but the core of the technique is always that random swapping creates signals carrying information on error parameters.

3.1.4.3 Rapid Calibration of ADC Errors

In an industrial environment where ICs are mass produced, ICs are tested for functionality by automated testers. In ADCs which use background-statistical techniques to achieve calibration, long calibration times can lead to excessive test times thus limiting IC production throughput and hence revenue. For example, with four million calibration cycles, even with a reasonably high sampling rate of 40 MS/s, one tenth of a second would be required at minimum to test each ADC. For higher resolution and/or lower speed ADCs the test time can be much higher [61]. In the interest of larger production throughput it is highly desirable to reduce calibration time. Reducing calibration time has become an active area of research over the past

few years. A calibration method which has proven to be highly effective in reducing calibration times in background schemes is the 'dual-ADC' or 'split-ADC' approach [61], [62],[63].

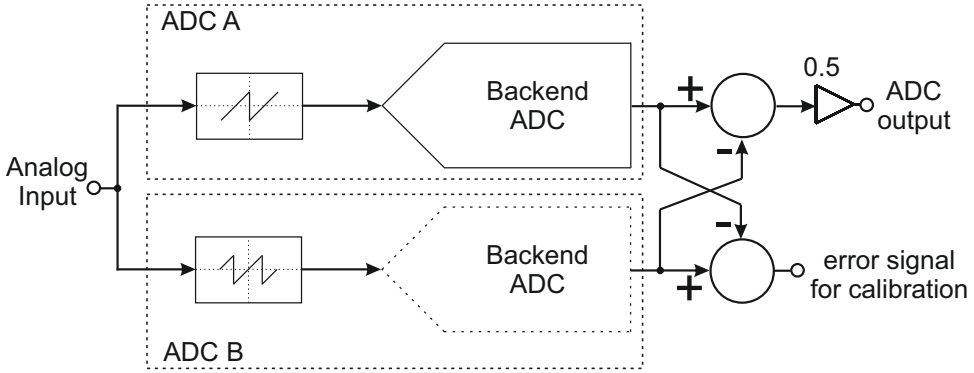

Figure 3.3. Split-ADC topology

As shown in 3.3 , the split-ADC takes a single ADC and splits it into two almost identical ADCs where each ADC has half the area, and half the thermal noise floor (thus half the power) of the overall ADC- The final ADC output is derived by taking the average of each ADC output, hence power and area of the split ADC topology to a first order are not increased over a conventional ADC [61]. Each ADC is identical, except the residue transfer curve of the stage under calibration in one ADC is designed differently than the other. As a result when the ADCs are free of errors both ADCs produce the same output, however when errors are included each ADC produces different outputs. Since the analog input effectively appears as common mode to the split-ADCs, the error signal which is formed by the difference of the two ADCs is very weakly correlated to the analog input. However the error sources are very highly correlated with the difference in ADC outputs (i.e. error signal) due to each residue transfer curve being designed slightly differently than the other signal [62]. Thus error sources can be estimated very quickly in the background by only looking at a small number of clock cycles of the error signal.

3.2 Calibration based on Volterra Kernel

Non-linear calibration for the pipeline ADCs enables better linearity and higher sampling frequency, correcting errors due to incomplete settling, slew-rate limitations, switches' and amplifier' non linearity asbdescribed in [64] and [65]. Volterra models can be adopted to represent weakly non linear effect for example for RF power amplifier.

3.2.1 Volterra Series

The Volterra series representation is a popular black-box macromodeling approach for describing nonlinear devices with memory [66] [67] . It can support timedomain simulation with arbitrary input and is valid for signals that can excite both linear and nonlinear responses. Without knowing the state equation, the difficulty in determining higher order Volterra kernels has restricted its application. Volterra Series has been widely used to characterize nonlinear systems with memory [68]. For a system with input $u(t)$, the output $y(t)$ can be expressed using the expansion

$$y(t) = \sum_{n=1}^{\infty} y_n(t) \tag{3.1}$$

with

$$y_n(t) = \frac{1}{n!} \int_{-\infty}^{+\infty} \cdots \int_{-\infty}^{+\infty} h_n(\tau_1, \ldots, \tau_n) \cdot u(t-\tau_1) \ldots u(t-\tau_n) d\tau_1 \ldots d\tau_n \tag{3.2}$$

where $h_n(\tau_1, \ldots, \tau_n)$ is the n_{th}-order time-domain Volterra kernel or impulse response. In particular, $y1(t)$ is the usual first-order convolution having its frequency-domain representation

$$Y_1(\omega) = H_1((\omega)U((\omega) \tag{3.3}$$

where $H_1((\omega) = \int_{-\infty}^{+\infty} h_1(\tau) e^{-j\omega\tau} d\tau$ is the linear transfer function or the first-order Volterra kernel. $U(\omega)$ is the Fourier transform of $u(t)$. However, the nonlinear higher order output cannot be written in a form similar to (3.3). By replacing the single time axis by multiple time axes, (3.2) becomes

$$y_n(t_1, \ldots, t_n) = \int_{-\infty}^{+\infty} \cdots \int_{-\infty}^{+\infty} h_n(\tau_1, \ldots, \tau_n) \cdot u(t_1-\tau_1) \ldots u(t_n-\tau_n) d\tau_1 \ldots d\tau_n \tag{3.4}$$

The frequency-domain representation of (3.4) can be conveniently written in a form similar to (3.3)

$$Y_n(\omega_1, \ldots, \omega_n) = H_n(\omega_1, \ldots, \omega_n) U(\omega_1) \ldots U(\omega_n) \tag{3.5}$$

with the nonlinear transfer function H_n defined as

$$H_n(\omega_1, \ldots, \omega_n) = \int_{-\infty}^{+\infty} \cdots \int_{-\infty}^{+\infty} h_n(\tau_1, \ldots, \tau_n) e^{-j\omega_1\tau_1} \cdots e^{-j\omega_n\tau_n} d\tau_1 \cdots d\tau_n \tag{3.6}$$

To restore $y_n(t)$, one then evaluates along the diagonal line in the multitime hyperplane

$$y_n(t) = y_n(t_1, \ldots, t_n)|t_1 = t_2 = \cdots = t_n = t \tag{3.7}$$

where $y_n(t_1, \ldots, t_n)$ is the multidimensional inverse Fourier transform of $Y_n(\omega_1, \ldots, \omega_n)$.

3.2.2 Volterra Calibration Survey

Volterra kernels [69] can be used to improve the linearity of mixed-signal circuits such as Sample-and-Hold stages [64], but the number of parameters to be estimated can be large, thus the computational cost can be too high. A possible solution can be use a subsets of Volterra kernels with a reduced number of parameters to model the nonlinearities, such as the nonlinear switch on-resistance [70], [71]. In [70] a performance improvement of more than 20 dB is achieved by using hundreds of coefficients, whereas without complexity reduction the number of parameters would have run into thousands. In [71] a model which reduces complexity down to tens of parameters is presented, they reach a linearity improvement of about 10 dB, up to close to 30 dB for larger models and using inherently more linear analogue circuit techniques such as bootstrap switches. These techniques are developed for a specific model of distortion and may thus be less effective in a more general case in which switch nonlinearities, amplifier nonlinearities, and incomplete signal settlings are present, which is often the case in low-power high-speed SHA stages. Moreover in [71] is shown that some circuital technique such as transmission gates switches are less disposed to calibration, and achieve lower linearity improvement. In [64], we show that Volterra kernels of limited complexity which use a specific lag for each order of nonlinearity, after careful pruning of the model to eliminate the parameters which add little to overall performance, achieve robust performance improvement.

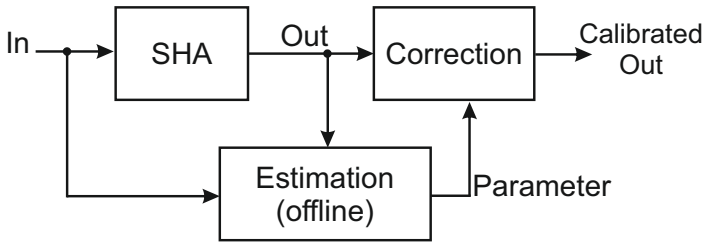

Figure 3.4. Block scheme of calibrated system

The schematic diagram of the calibrated system is shown in figure 3.4, the output of the Sample-and-Hold is taken as input by a digital block of correction which processes the signal to maximise the linearity at its output. The processing operated by the correction block depends on a set of parameters which are estimated during

an Estimation phase which is performed offline. The estimation phase consists in applying a set of know test signals at the input of the Sample-and-Hold to find the optimal set of parameter. More precisely each test signal is a sinusoid, and its frequency is changed from about DC to about the Nyquist frequency to cover the whole bandwidth of the SHA, as in [72].

3.2.3 Pruned Volterra Calibration

Model complexity is the most limiting factor in the applicability of the Volterra models. An a posteriori approach to reduce the computational complexity should be used as in [69].

A Volterra kernel is defined by an order O and a lag L, and a Volterra model is a set of Volterra kernels of different orders. Given an input x, the output of a Volterra kernel is

$$y_{OL(O)}(n) = \sum_{i_1=0}^{L} \sum_{i_2=i_1}^{L} \cdots \sum_{i_O=i_{O-1}}^{L} h^{O}_{i1,i2,\cdots,i_o} \Psi \tag{3.8}$$

$$\Psi = x(n-i_1)x(n-i_2)\cdots x(n-i_O) \tag{3.9}$$

We define the lag L as a function of O, meaning that for each order there is a specific lag. Since the number of terms in (3.8) rapidly increases with O and L, keeping small lags for high-order kernels is of the essence to avoid an explosion of the computational cost. When $O = 1$, the Volterra kernel is an FIR filter of coefficients $h^1_{i_1}$. $O = 0$ is the offset term. If the system is fully differential, the even-order distortions are usually small; in the following, odd-order kernels are mainly used, and it is shown that only a few even-order terms are needed when mismatch is included in Monte Carlo simulations.

3.2.3.1 Pruned Volterra Sample-and-Hold

A symmerical Volterra kernels are adopted to model a Sample-and-Hold circuit. The simulated circuit is a fully differential flipped-around Sample-and-Hold (as shown in figure) with a folded cascode amplifier and transmission gate switches, the technology node used is the CMOS 40nm provided by STmicroelectronics.

The schematic of the folded cascode ota is shown in figure 3.6. The OTA has been designed for achieve a gain of 36dB and a f_u of 250MHz. The total power consumption of the OTA is $30\mu W$.

The fully differential amplifier makes use of a Common Mode Feedback circuit that exploit the switched capacitor technique to stabilize the common mode output voltage to the desired value. The involved amplifier has an open-loop gain of 36 dB and a gain-bandwidth product of 250 MHz, and consumes 30 μW. The Sample-and-Hold circuit is clocked at 50 MSps, and settling is incomplete at this speed.

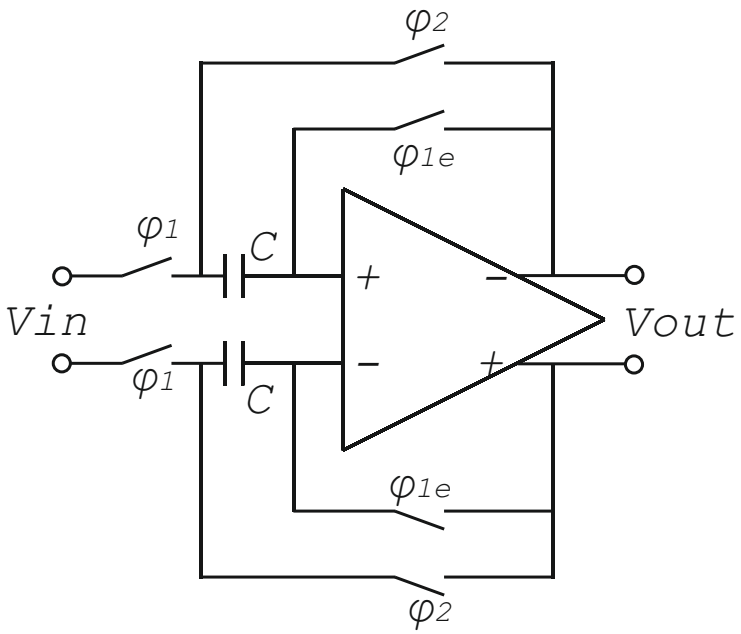

Figure 3.5. Flip-around Sample-and-Hold schematic

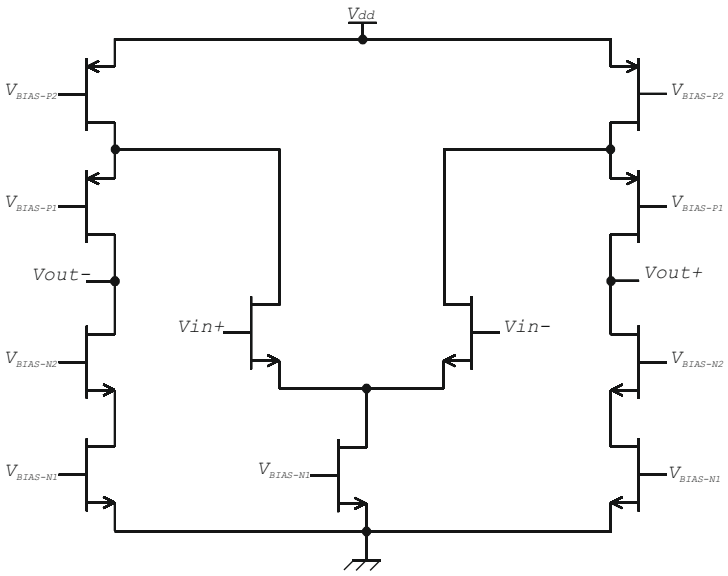

Figure 3.6. Folded cascode OTA

The supply voltage is 1.2 V and signals are 0.6 V peak, differential. No analogue techniques to improve accuracy have been employed. A total of 30 input frequencies have been simulated in the first Nyquist band:

$$s_{in,j}(t) = Asin(2\pi f_j t) \tag{3.10}$$

with $f_j = \frac{j}{64} f_s, \in \{1, 31\} \wedge j \neq 16$ The frquency $f_s/4$ has not been used because all of its odd harmonics fall on $f_s/4$ itself due to aliasing and all the even harmonics fall to DC. Each test signal has 80 samples, the first 16 used to reach steady-state behaviour. Of these signals, 22 have been used to estimate the parameters, and 8 have been used for out-of-sample validation of the robustness of the technique: linearity improvement is similar for in-sample and out-of-sample tones, implying robust performance improvement also for signals not included in the calibration set.

An iterative procedure has been introduced to reduce the number of parameters, and consequently the computational cost. Starting from the full Volterra model, the element which impacts linearity the least is removed. The procedure is repeated until linearity or gain flatness is no longer acceptable (parameters are recalculated at each iteration). Some pruning usually increases linearity. This result is counterintuitive, but can be explained in that the Volterra model has a linear and several nonlinear sections. By the theory of least-squares estimation, the overall error increases with pruning, but sometimes pruning increases the linear error, reducing gain flatness, while improving linearity. Pruning also reduces numerical inaccuracy due to collinearity in the least-squares estimation by removing highly-correlated components which have little impact on the residual error. By deep pruning, reduction by a factor of 2 or 3 of the number of parameters has been achieved without loss of linearity.

3.2.3.2 Simulation Results

In the following, simulations are reported with a lag structure (L_1, L_3, L_5, L_7), implying that the lag of the kernel of order k is L_k. To account for mismatch effects in Monte Carlo simulations, which create even-order distortions, terms of order 0 (offset), 2 and 4 have been added, with $L_0 = L_2 = L_4 = 0$; a constant term and two terms $x^2(n)$ and $x^4(n)$ are sufficient for correction at a computational cost of three additional multiplications. More complex even-order kernels do not improve linearity. Linearity improvement has been defined as the difference between the minimum of the signal-to-noise-and-distortion ratio after and before calibration in a specified band. Gain flatness is the variation of the linear gain in the same band.

Figure 3.7 shows that an improvement of 20 dB on SFDR can be obtained from DC to 80% of the Nyquist band with lags (20, 2, 2, 2). There are 87 coefficients to estimate, and gain flatness in the band of interest is below 0.01 dB.

Figure 3.8 is that for lags (20, 4, 2, 2), with 108 free coefficients. Out-of-sample frequencies are shown using markers. The simulations do not include noise, so

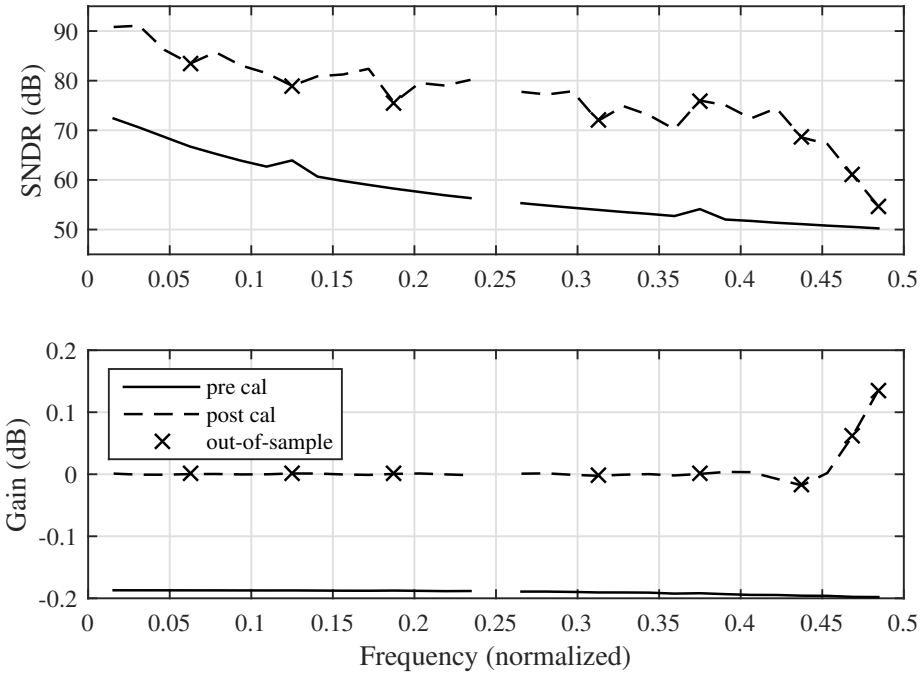

Figure 3.7. Pre and post calibration comparison, using a lag configuration = [20,2,2,2].

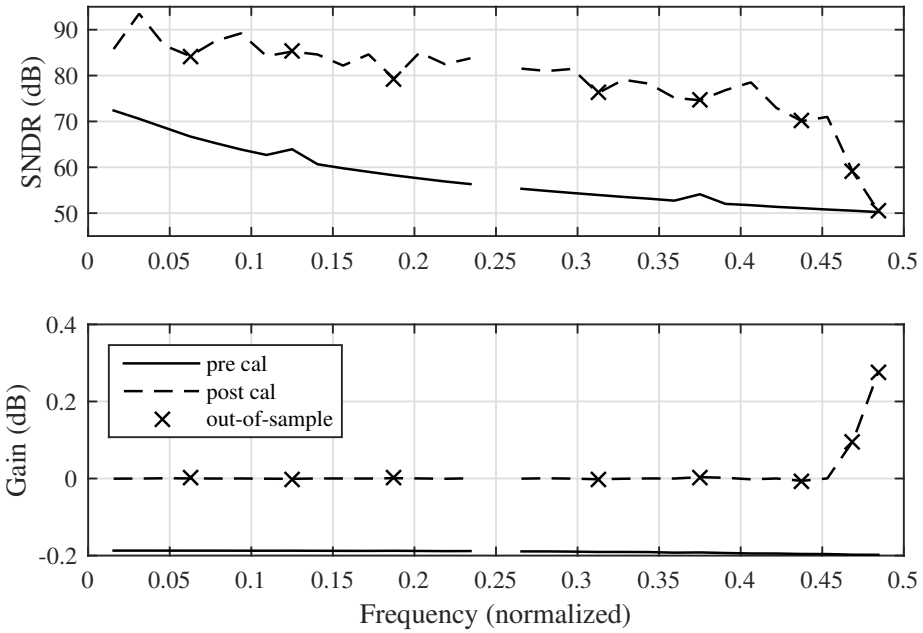

Figure 3.8. Pre and post calibration comparison, using a lag configuration = [20,4,2,2].

that $SNDR = -THD$, the total harmonic distortion. Calibration cannot improve the signal-to-noise ratio, and noise would only increase the duration of the offline

Estimation phase.

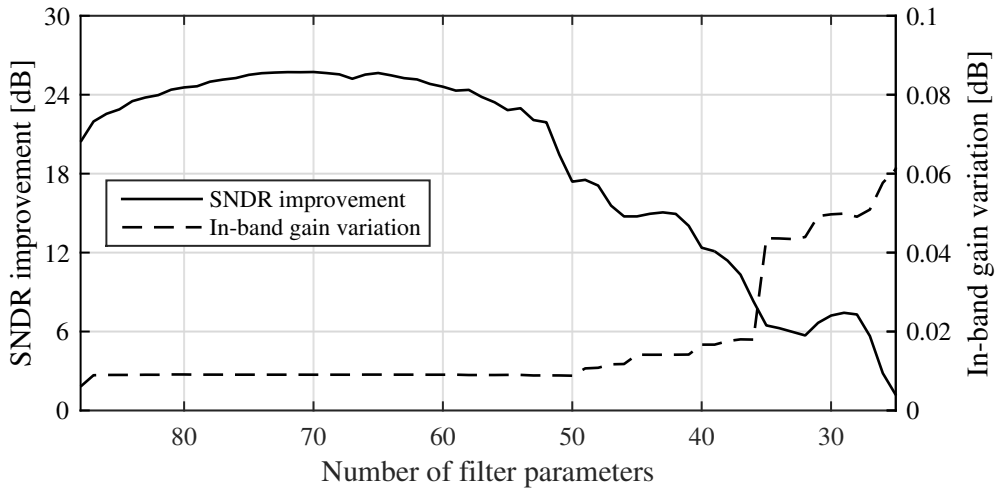

Figure 3.9. SNDR improvement and gain variations with pruning, starting from [20,2,2,2] lag configuration

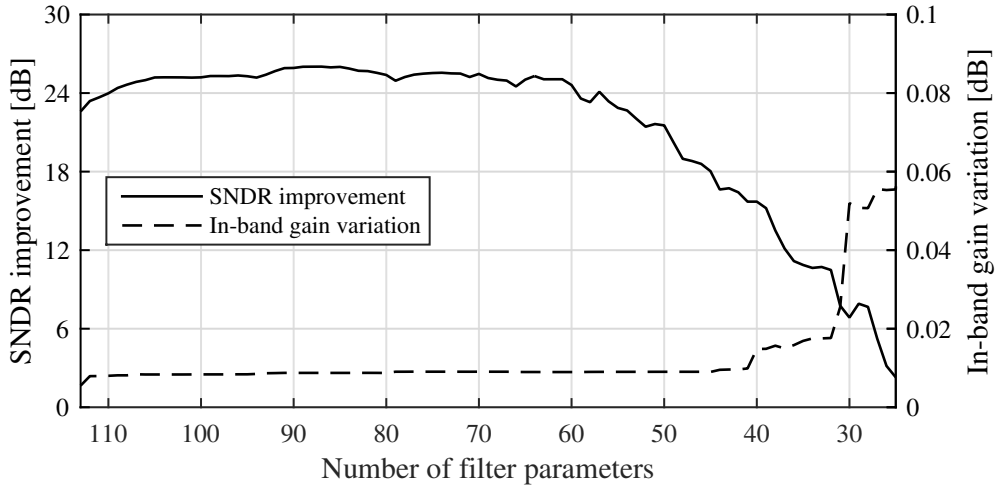

Figure 3.10. SNDR improvement and gain variations with pruning, starting from [20,4,2,2] lag configuration

Figures 3.9 and 3.10 show the effect of pruning. Starting from the largest number of parameters given the initial lag structure, removing a few parameters improves both linearity and computational cost, and a large reduction in the number of parameters can be achieved preserving the same linearity gain obtained without pruning. Figure 3.9 shows that the number of parameters can be reduced up to 39, keeping more than 12 dB of improvement, starting from lags (20, 2, 2, 2). The peak linearity improvement is 25.7dB with 70 parameters. Figure 3.10 shows that a peak linearity gain of 24 dB can be achieved with 57 parameters, starting from lags (20,

4, 2, 2). Since the minimum number of coefficients for a given SNDR improvement varies with the initial lag structure, many simulations have been performed to achieve a given improvement with a minimal number of coefficients. Results show that 17 parameters are enough to gain 6 dB, 21 for 12 dB, 36 for 18 dB, and 53 for 24 dB.

Out-of-sample data have been used to test the algorithm's performance with signals not used in estimation. There is no significant difference between in-sample and out-of-sample frequencies. Temperature and voltage variations have been tested. Offline calibration techniques need the calibrated system to be stable against operational conditions because parameters are kept constant after estimation. Temperature variations of ±10°C and supply voltage variations of ±1% (12 mV) have little effect, especially for simpler models.

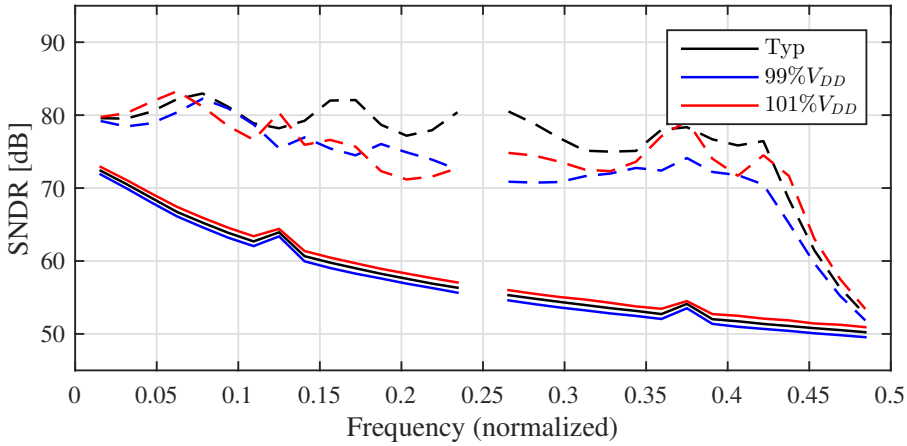

Figure 3.11. Pre and post calibration comparison with ±1% voltage supply variations using 54 parameters pruned model

In figure 3.11 the post calibration SNDR of the typical case against the voltage supply variation is- shown. The mean improvement is 23dB, in the worst case the improvement is 18.5 dB when 99%VDD is applied.

Parameter sets optimised for different operating conditions may be stored in a look-up table, increasing the operational range. Monte Carlo simulations show that a limited number of even-order correction terms (three including offset) are sufficient.

3.2.3.3 Pruned Volterra ADC

The calibration of non-linear effect in pipeline ADC allows to reach high linearity and fast conversion frequency through the correction of errors due to incomplete settling, slew-rate limitations and memory effect in switched capacitors circuits. The calibration method [64] proposed to increase the features of the sample and hold stage, can be extended to pipeline ADCs, and its performance advantage increases

with the sampling frequency of the ADC. This approach achieves better linearity with comparable complexity than other simplified Volterra models found in the literature.

Model complexity is a limiting factor in the applicability of Volterra models. An a posteriori approach to reduce the computational complexity of Volterra models was applied in [69] to a SHA stage. For each kernel order, a specific memory length was chosen, and an iterative pruning technique was then used to further reduce complexity. The literature on ADC calibration usually employs a different approach. Volterra kernels used for generic ADCs are based on a priori hypotheses on the structure of the kernel [70], [72], [73] to reduce the number of parameters. We show that these approaches may be less effective, and sometimes ineffective, for the calibration of high-speed pipeline ADCs.

The model is applied on a pipeline ADC composed by 1.5-bit MDAC stages. Radix-based calibration [4] has been used to correct errors in pipeline ADCs such as finite gain and capacitor mismatch [74]. Only the output of the pipeline ADC (after conventional calibration) is used in our non-linear calibration technique. This makes this technique suitable for calibrating off-the-shelf components, as it does not require modifications in the ADC hardware [72].

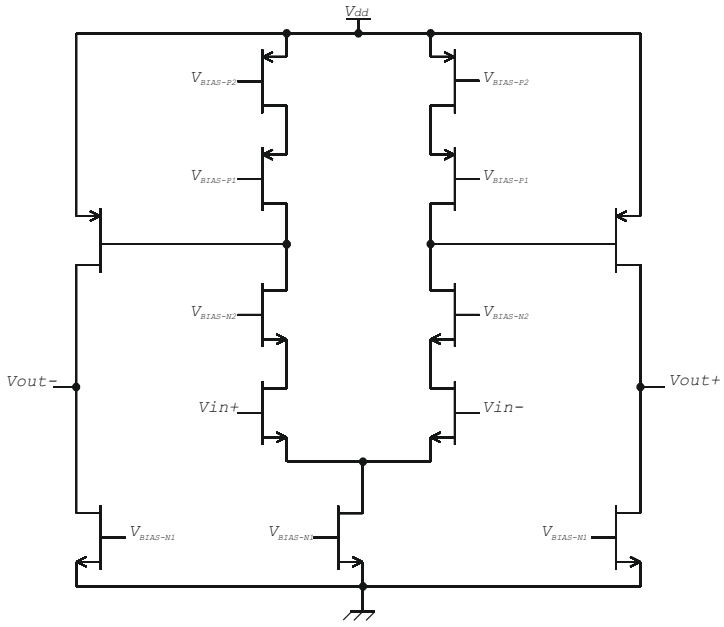

Figure 3.12. Schematic of telescopic OTA

The simulated ADC has a Sample-and-Hold stage and 16 1.5-bit MDAC stages. The amplifier is a two-stage Miller-compensated operational transconductance amplifier (OTA) with a telescopic cascode as first stage as shown in figure 3.12. The telescopic has been designed with a gain equal to 68dB, a GBW of 1GHz and 34° of phase margin. The total power consumption for each telescopic OTA is 1.64mW.

Reference voltages are buffered, with one buffer per stage. Each stage has a common-mode feedback with resistive-partitioning and a diode-loaded differential pair. All the switches are transmission gates. The reference voltage is 1 Vpp differential. The integrated circuit was simulated in the CMOS 40 nm STMicroelectronic process, with 1.2 V power supply. The power dissipation of the ADC is 30 mW. The pipeline ADC was originally designed for a conversion frequency of 50 MSps, but it has been pushed up to 125 MSps, thanks to digital calibration. Power consumption does not change appreciably with the clock frequency. The ADC's signal-to-noise-and-distortion-ratio has been defined as that of the tone from DC to 80% of the Nyquist frequency with the highest distortion. All the 30 frequencies are considered: if the model overfits the data, out-of-sample tones have lower SNDR. Figures 3.14 and 3.13 show results for kernels described as L1, L3, L5, ..., L19 (only odd-order kernels are included [69]). The nominal resolution of the pipeline is the number of MDAC stages plus 1.

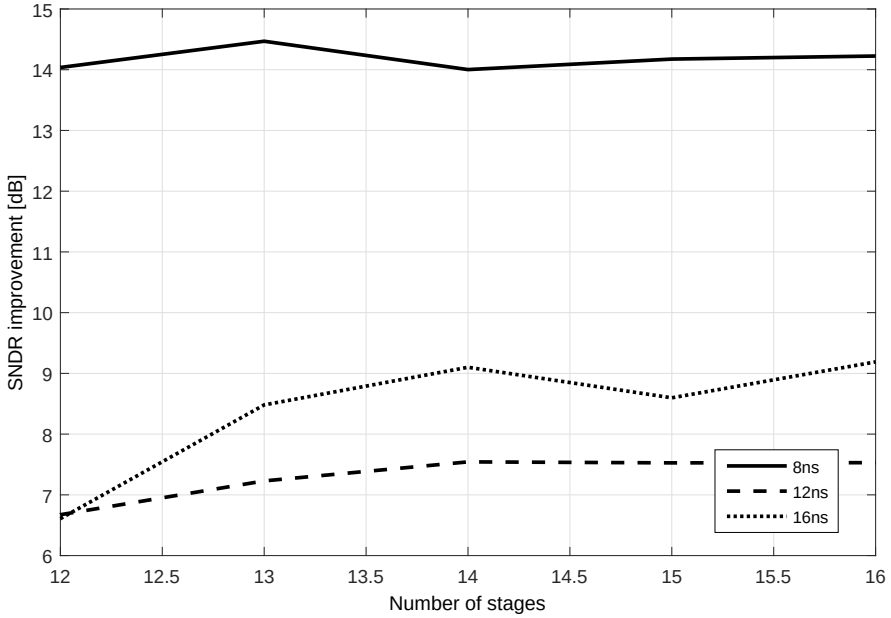

Figure 3.13. SNDR improvement against nominal ADC resolution and sampling period, starting with lag structure $\{30, 4, 2, 2, 1, 1, 1, 0, 0, 0\}$ for odd orders from 1 to 19. Number of parameters is 162 without pruning.

The Volterra model has been used to simulate both the improvement in the SHA stage alone (assuming an ideal ADC) and of the whole ADC. The ADC has about 9 bits of ENOB before calibration and close to 11.5 after. The SHA's ENOB is 10.5 bits and reaches 14 bits after calibration. A memoryless polynomial model with odd-order kernels from 3 to 19 has been simulated: it improves linearity by 0.5 bit at 16 and 12 ns of clock frequency, but it has no effect at 8 ns (125 MSps). Pruning improves linearity, initially, and reduces model complexity by a factor of

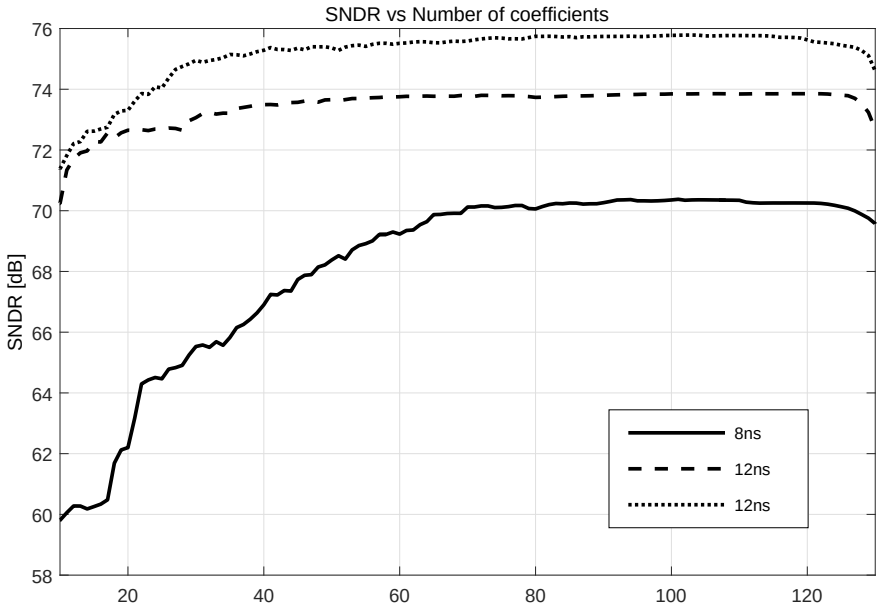

Figure 3.14. SNDR against pruning and sampling period, starting with lag structure $\{30, 4, 2, 2, 1, 1, 1, 0, 0, 0\}$ for odd kernels from orders 1 to 19

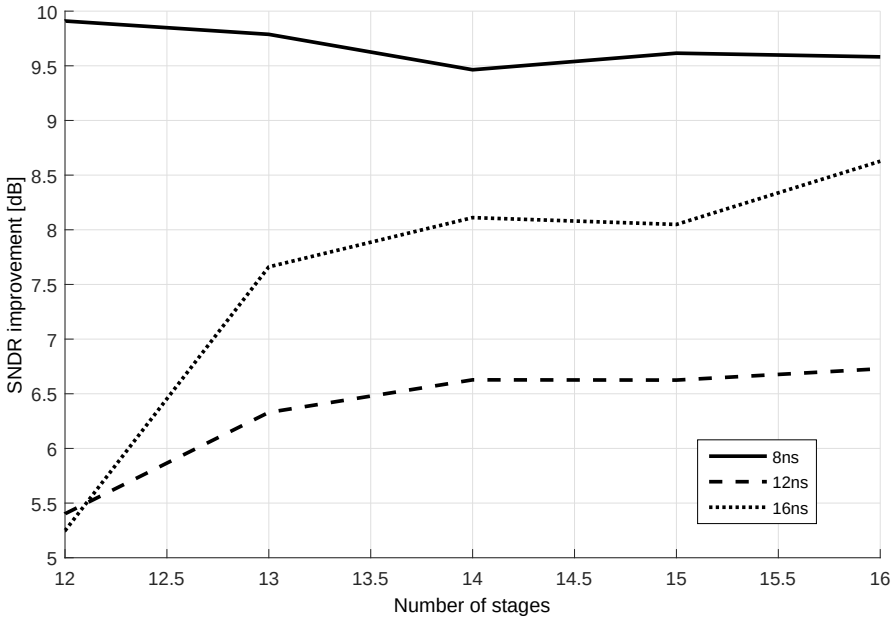

Figure 3.15. SNDR improvement against nominal ADC resolution and sampling period, starting with lag structure $\{30, 3, 2, 1, 0, 0, 0, 0, 0, 0\}$ for odd orders from 1 to 19

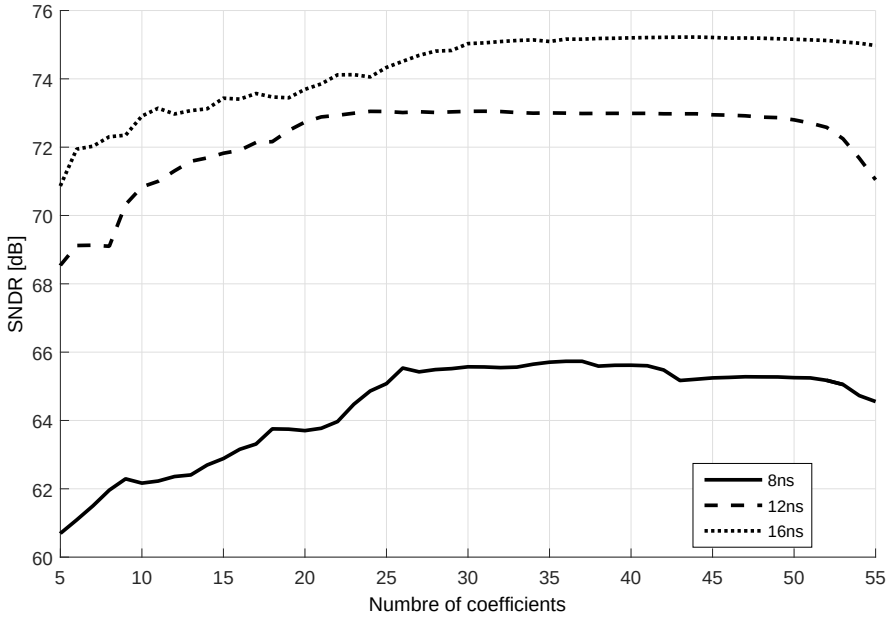

Figure 3.16. SNDR against pruning and sampling period, starting with lag structure $\{30, 3, 2, 1, 0, 0, 0, 0, 0, 0\}$ for odd kernels from orders 1 to 19

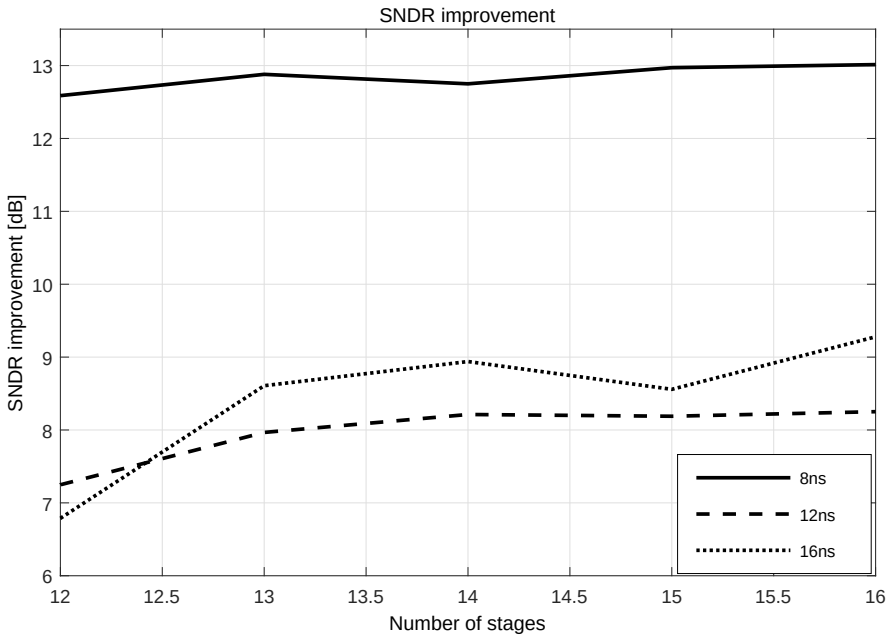

Figure 3.17. SNDR improvement against nominal ADC resolution and sampling period, starting with lag structure $\{30, 5, 3, 1, 0, 0, 0, 0, 0, 0\}$ for odd orders from 1 to 19

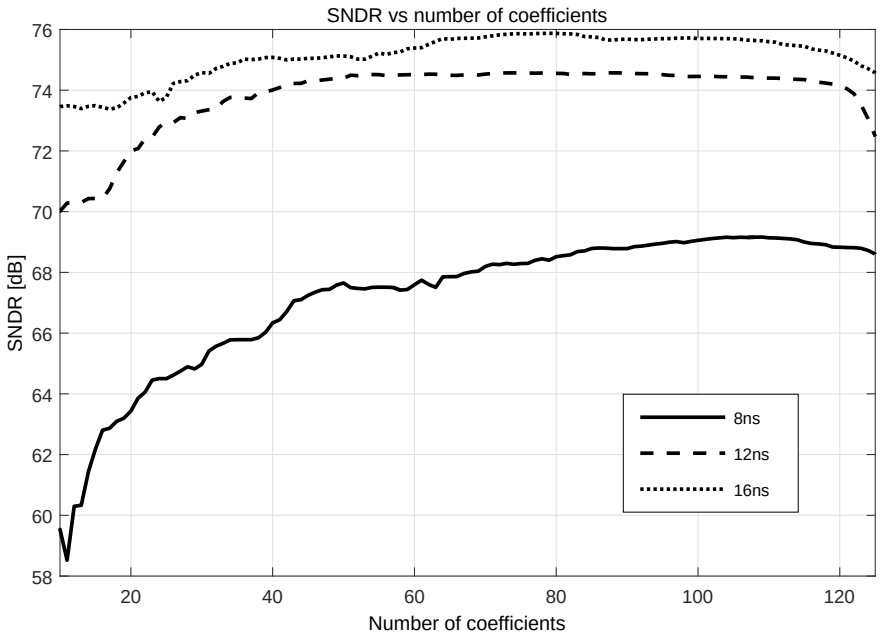

Figure 3.18. SNDR against pruning and sampling period, starting with lag structure $\{30, 5, 3, 1, 0, 0, 0, 0, 0, 0\}$ for odd kernels from orders 1 to 19

about 2. The models in [70], [73], and in [72], [75], [76] have been used to calibrate our 8 ns sampling time dataset. Table 1 reports the best results we have found for each algorithm. The model [73] is simple but not effective. The MP model in [72] has limited effectiveness (about 0.5 bit peak improvement), with a low parameter count. The MGMP model is marginally better, but more complex. The model in [70] is more effective, yielding a maximum improvement of about 1.2 bits with 205 coefficients, and about 0.9 bit with 21 coefficients. ENOB improvement saturates at 1.2. Our pruned Volterra model achieves performance improvements larger than 1.

Conclusion: Starting from a Volterra model with odd-order kernels, and lengths dependent on the kernel order (shorter high-order kernels and longer low-order kernels), we have applied the iterative pruning technique to a switched capacitor pipeline ADC. The ADC was designed to work at 50 MSps, but was simulated at 66.7, 83.3, and 125 MSps to determine the effectiveness of the calibration technique in correcting for heavily non-linear incomplete signal settling. We have then compared our calibration technique, using our 125 MSps dataset, with others reported in the literature. Our approach is shown to be more effective, reaching higher linearity with comparable complexity. Pipeline ADCs, as opposed to SHA front-end stages, are heavily nonlinear because their input–output characteristic depends on the sub-ADCs inside the MDACs (two comparators in the case of 1.5-bit stages) [77]. Volterra models are thus less effective for the ADC as a whole and larger models are required to achieve a given linearity improvement. Despite this, a performance improvement

Reference	Max order	Length	Complexity	ENOB
[73]	3-19	-	-	0
[70]	5	3	21	+0.9
[72]	9	20	205	+1.2
[72] (MP)	5	2	6	+0.5
[72] (MGMP)	9	4	20	+0.4
[72] (MGMP)	11	5	30	+0.7
[72] (MGMP)	Fig. 3.13		53	+1.5
[72] (MGMP)	Fig. 3.13		72	+2.0
[72] (MGMP)	Fig. 3.13		101	+2.5

Table 3.1. Linearity improvement and complexity for various models

between 6 and 15 dB is possible, with models from 37 to 101 coefficients. Even-order distortions are usually lower than odd-order ones in fullydifferential structures, and in [64] a few additional even-order terms were sufficient to correct them. It is possible to enhance performance for pipeline ADCs driven at much higher sampling frequencies than the nominal one, as the Volterra model can correct for the effects of the non-linear dynamics of the circuits. The performance improvement is in fact particularly significant for the largest simulated sampling frequency of 125 MSps.

Chapter 4

Reconfigurability

In a wide range of applications such as audio signal processing, digital image processing, speech processing, digital communications, radar, and biomedicine, the involved signals are digitally treated through Digital Signal Processing (DSP) techniques. The DSP algorithms are implemented in ASICs (Application Specific Integrated Circuit) or FPGAs (Field Programmable Gate Arrays). Generally the DSP algorithms can be executed economically with general purpose CPUs, but for real time applications, specific DSP-core are required, based both on fixed point or floating point arithmetic. Before digital processing operations, the input signal should be treated and conditioned by an analog front-end composed by operational amplifiers, filters and sometimes Radio Frequency (RF) circuitry. A mixed-signal block that takes an analog input and provides as output a representation in digital domain is required to merge the analog and digital worlds, this joining ring is the Analog-to-Digital Converter (ADC). A wide range of conversion structures was developed to optimize different charateristics related to the system requirement, such as the conversion speed, resolution, power consumption and area occupation. Reconfigurable charateristics make the ADC suitable for a broad number of application where the requirements for the subcircuits are variable during the operation, or in general the circuit behaviour can be reconfigured. One application where reconfigurable ADC are suitable are the micropower sensor networks, that have a broad range of applications such as environmental monitoring, chemical detection and medical monitoring systems [78].

We can consider a medical monitoring system as example to illustrate the typical structure of a sensor node. As seen in Figure 4.1 a typical medical monitoring system consists of multiple sensors, a low noise instrumentation amplifier (IA), an analog to-digital converter (ADC) and a digital signal processor (DSP), evenually a RF front-end is used to send the processed data to a node that collects all the data that are provided from the nodes of the network. The design of the system is primarily constrained by area and power. Small die area helps to achieve a small form factor,

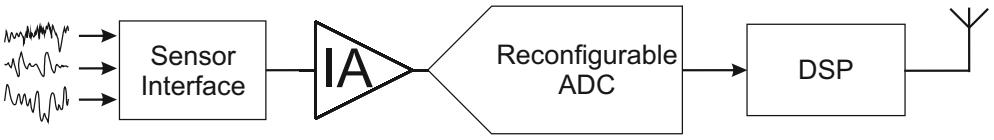

Figure 4.1. A typical medical monitoring system consisting of a sensor interface with multiple sensors, instrumentation amplifier, ADC, DSP and a short range radio.

Bio-potential	**Bandwidth [Hz]**	**Amplitude**
EEG (electroencephalography)	0.5 ÷ 40	0.5 ÷ 100 μV
ECG (electrocardiography)	0.05 ÷ 100	1 ÷ 5 mV
EMG (electromyography)	20 ÷ 2000	1 ÷ 10 mV
EOG (electrooculography)	0 ÷ 10	10 ÷ 100 μV
ERG (electroretinography)	1 ÷ 100	0.5 ÷ 8 μV
ECoG (electrocortigraphy)	0.05 ÷ 200	5 ÷ 100 μV
LFP (local field potential)	0.05 ÷ 100	10 μ V ÷ 1 mV
ENAP (extracellular neural action pot.)	0.1 ÷ 10000	50 ÷ 500 μ V

Table 4.1. Bandwidths and amplitudes of various bio-potentials.

while low power consumption is crucial in extending the lifetime of the system, in fact, usually the sensors nodes are battery powered or use harvested energy, thus a single high-efficuency ADC is used to reduce the power consumption. Each node of the net takes as input different analog inputs, in term of amplitude and bandwidth. Thus the analog front-end, and the ADC performance must be variable to follow the requirements due to the signal, in fact in order not to waste a large amount of energy in this application the sampling frequency of the ADC is always set to the minimum value that avoids aliasing phenomena. Reconfigurable circuits are very useful in the medical monitoring system because many medical applications require the acquisition of bio-potentials, or physiological signals, which often have different amplitudes and bandwidths [79], [80], [81]. Common bio-potentials and their characteristics are listed in Table.

In order to minimize design time and die area, as well as maximizing the number of applications, the analog front-end should be able to adjust its gain and bandwidth to accommodate a wide range of bio-potentials. In particular, to minimize the power consumption, the ADC should also be reconfigurable and be able to scale its performance depending on the application. In the considered system, the dynamic range of the analog front-end should be large enough to cover the whole signal amplitude range to be detected. Assuming that the instrumentation amplifier and

front-end filters are designed for a sufficient dynamic range, the ADC will limit the dynamic range of the system by introducing quantization noise and distortion to the signal, moreover, the ADC's resolution should be chosen sufficiently high to provide an adequate signal-to-noise and distortion ratio (SNDR). From table 4.1, it can be seen that the signal amplitude range differs for each bio-potential, suggesting different ADC resolution requirements. For a correct choosing of the ADC's resolution, other considerations must be taken into account. Taking the ECG as an example application, simple tasks such as heart frequency extraction requires no more than 8-bits [82]. However, more complex algorithms used in ECG for detecting slow changes in the ST pattern (figure 4.2) may require 12 to 16-bits of resolution [83].

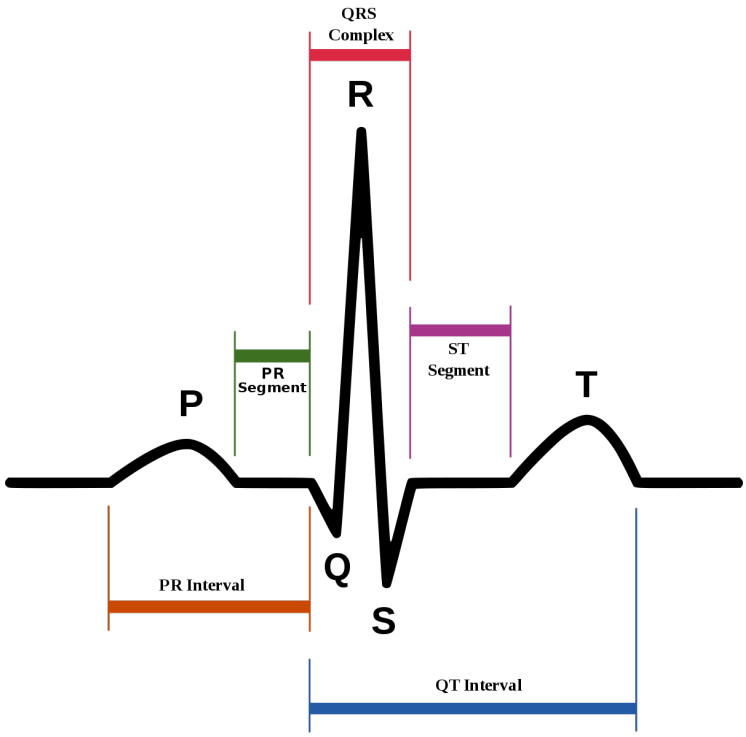

Figure 4.2. Scematic representation of normal ECG

The simplest approach would be to design the ADC for the worst stringent resolution requirement and truncate the ADC outputs as needed. But this solution is very inefficient in term of energy efficiency because power consumption in ADCs typically scales exponentially with the effective resolution. Thus, to increase the flexibility in the detectable signal amplitude range and processing algorithms, an ADC with reconfigurable resolution is highly desired. Moreover, signal bandwidths for bio-potentials differ across applications, also the maximum sampling rate must satisfy the Nyquist requirement for the highest bandwidth application. However, since it is well known that power consumption scales with frequency in any digital

or mixed-signal system, it is desirable to be able to reduce the sampling rate for all those applications that have low bandwidth constraints. For medical applications, the bandwidth of biopotentials are typically very low (up to a few kHz) and the ADC sampling rate can be as low as just tens of kilo-Samples per second. In the proposed design, a maximum sampling rate of 100-MS/s was chosen to demonstrate frequency scaling over a larger range of frequencies. This will make the ADC suitable for different application such as telecommunications and wireless sensors network, indeed, another important application where is required the reconfigurability of the circuits are the Software-Defined Radio (SDR). A SDR is a transceiver system in which most of the signal processing is done in the digital domain. In order to massively employ digital signal processing, SDRs have to use ADCs, in the RX part, and DACs (digital-to-analog converters) in the TX part, and to push these components as close to the antenna as possible. SDR circuits must be reconfigurable to handle diferent communications standardands such as GSM, UMTS, 802.11, HIPERLAN, Bluetooth, and to use adaptive techniques to optimize the behaviour of the radio system in varying operating and environmental conditions. One of the main advantages of SDR is the capability of handling multiple standards on a single architecture. This is due to the high flexibility inherent in programmable devices, even though the radio-frequency section and the data converters cannot be made as flexible as the digital processing section. However, Adaptive SDR may be capable of increasing flexibility even more by using tunable RF circuits and reconfigurable ADCs. For both the applications reported as example a critical role is played by the ADC, because it sets the linearity of the overall system, and also is one of the main power consumption sources. A pipelined architecture for the ADC is choosen in order to cover all the possible conbination of requirements in the parameter space composed by conversion frequency, resolution and signal amplitude.

4.0.1 Reconfigurable ADC Survey

A number of reconfigurable pipelined ADCs are reported in literature, most of them are reconfigurable only over bandwidth, while maintaining a constant 10-bit [84], [85], [86], [87],[88] or 12-bit [89] resolution. Alternatively, a reconfigurable ADC is presented in [90] that is reconfigurable over resolution only, while having a constant bandwidth. However, very few prevously reported pipelined ADCs are reconfigurable over both bandwidth and resolution [91], [92]. Altough these ADCs have a large bandwidth-resolution reconfigurability space, their efficiency is poor (pJ/conv-step) [91], [92]. Reconfigurable ADCs have also been proposed [93], [94], [95], [96], [97], [98], [99], [100] [101], [102] for specific bandwidth-resolution to cover specific radio standards. However, compared to pipelined ADCs, these ADCs do not usually cover a continuous reconfigurability range of bandwidths and resolution independently.

Author	Year	Technology	Resolution	f_S [MHz]	FOM
M. Anderson et al.	2005	180nm	6-12	-	2-107
W. Audoglio et al.	2006	130nm	6-10	20	0.9-5.1
G. Geelen et al.	2006	90nm	10	25-120	0.5-0.7
B. Xia et al.	2006	250nm	10	11-44	0.6-1
Y.-J. Kim et al.	2007	130nm	10	10-100	0.6-1.5
I. Ahmed et al.	2008	180nm	10	0.164-50	1.5-6
I. Ahmed et al.	2005	180nm	10	0.001-50	1.5-29
T. N. Andersen et al.	2005	180nm	12	20-110	0.66-0.8
M. Taherzadeh et al.	2013	90nm	10-12	0.4-44	0.35-0.5
M. C. Huang et al.	2010	180nm	10	0.1-100	0.5

Table 4.2. Reconfigurable ADC Survey

4.0.2 Voltage Scalable OPA

The block that plays the most critical role on the efficiency of an ADC pipeline, and also in many other analog-to-digital structures is the operational amplifier. The choice of the opamp's structure is driven by the constraints of the system, and also by the technology performance where the converter is implemented. For example, in low voltage applications all the stacked structures must be discarded to avoid limitation on the dynamic range of the signal. Moreover other constraints can be due to the circuital requirements, as in switched capacitors circuits where high driving current is required to obtain a fast charge of the capacitors, that should be made large to mimimize the effect of mismatch and to limit the effect of the thermal noise. Commonly also the total power consumption is a limitation, thus an extremely low static current is allowed in low power contexts. In a reconfigurable voltage-scalable ADC the opamps must be capable to operate with different voltage supply values, possibly keeping high level of gain, because the gain error of an MDAC is directly related to the gain of the opamp, that has therefore to be the highest possible. Summing up all the aforementioned requirements, we need an operational amplifier providing high gain (to guarantee high accuracy and low gain error in the SHA and MDAC, and thus low distortion in the pipeline ADC), low power consumption and short settling time (that determines the maximum sampling frequency). All these properties have to be maintained when supply voltage is scaled down. Obviously, a reduction of supply voltage results as an increase of settling time, that is fully compatible with our goal of scaling down supply voltage according to sampling frequency. A reduction of dynamic range is also obtained, but it can be coped with by using suitable modifications of the SHA architecture (e.g. [103]). In order to limit the static power consumption and achieve a high efficiency, a class-AB amplifier can

be used. Indeed class-AB operational amplifiers improve power-efficiency by enabling fast driving of large capacitive loads with low quiescent currents. This is important in low-voltage low-power applications ([104], [105], [106],[107]) , especially in CMOS integrated circuits where the load of one stage is often a capacitor. By improving the peak current, the quiescent current can be made low, thus reducing static power consumption. A limitation on the choice of the operational amplifier architecture is due to the low value of supply voltage, that in fact excludes all possible stacked solutions. The simplest gain stage that operates in class-AB is the CMOS inverter which usually is used in digital circuits, but can be used as a basic building block for realizing a pseudo differential structure operating in class-AB. This choice allows to decrease the value of power supply voltage, and at the same time allows to obtain a constant voltage gain over a wide range of power supply voltage values; in addition, it gives a large dynamic voltage range. Inverter-based operational amplifiers have already been presented in the literature [108],[109], and the schematic is reported in figure 4.3

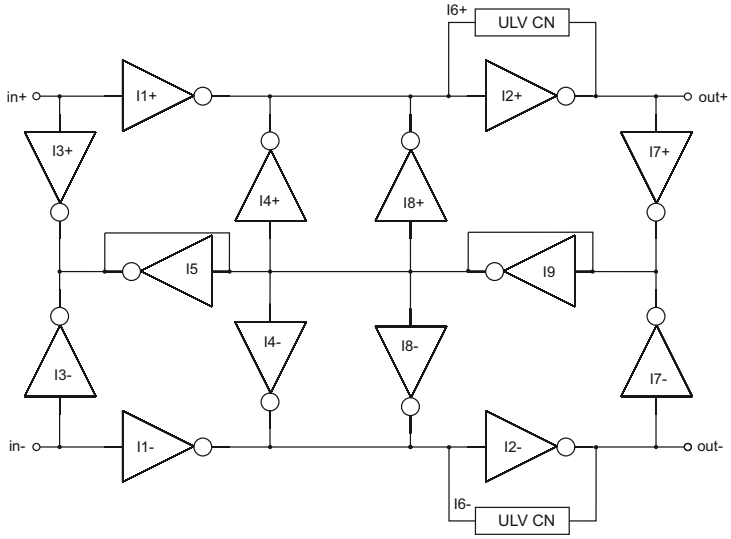

Figure 4.3. Inverter based two stage pseudo differntial opamp

The amplifier is a pseudo-differential, two stage amplifier. The inverters noted as $I1\pm$, $I2\pm$ work as gain stages, while inverters $I3\pm$,$I4\pm$ $I5\pm$ and $I7\pm$, $I8\pm$, $I9\pm$ realize respectively the common mode feed forward (CMFF) and the common mode feedback (CMFB). But in this amplifier they make use of body voltage control to set the dc current or the static output voltage. The way used to generate the controlling body voltage pose a limitation on the maximum supply voltage, in fact, as shown in figure 4.4, the body terminals of both NMOS and PMOS of the CMOS inverters in the reference circuit are connected toghether, thus the maximum supply voltage can not be higher than a diode forward voltage V_γ of about 0.6V. This control imposes

a limitation on the maximum supply voltage, thus making scalability difficult. To overcome this limitation we have applied a different solution that doesn't involve body bias, but exploits the feedback loop to set also the dc output voltage.

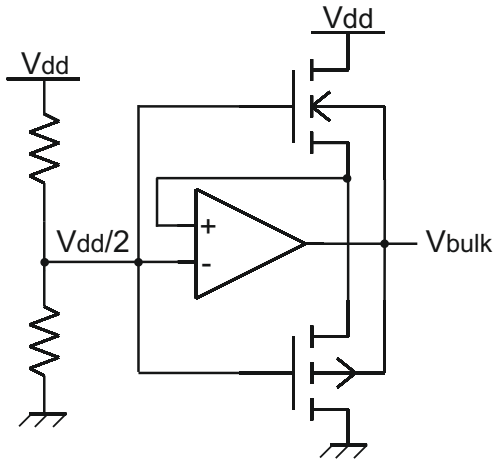

Figure 4.4. Body bias generation circuit

The CMOS inverter has been chosen as building block to develop a voltage-scalable pseudo-differential operational amplifier, because it is the simplest architecture of amplifier that operates in class-AB that allows the dynamic reduction of the supply voltage

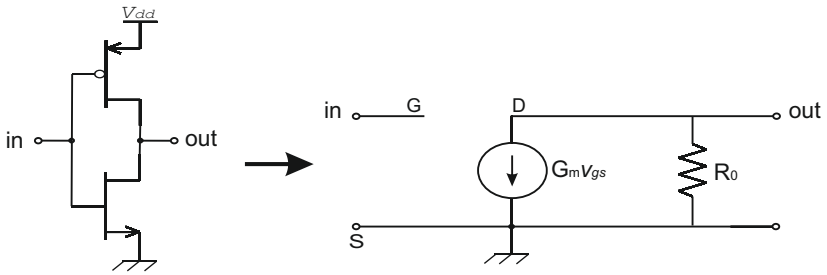

Figure 4.5. Small signal model of CMOS inverter

The small signal model of the inverter shown in figure 4.5 can be used in analog applications to determine voltage gain and bandwidth. The total transconductance, output resistance and input capacitance of an inverter stage can be derived from the simple model of PMOS and NMOS transistors, and are equal to: $G_m = G_{m_N} + G_{m_P}$; $r_0 = r_{0_N} || r_{0_P}$ and $C_g = C_{g_N} + C_{g_P}$ respectively, where G_{m_N} (G_{m_P}), r_{0_N} (r_{0_P}) and C_{g_N} (C_{g_P}) denote the transconductance, the output resistance and the gate capacitance of an NMOS (PMOS).

The pseudo-differential amplifiers are composed by two parallel single-ended amplifiers. Each of them processes a signal with the same amplitude but opposite

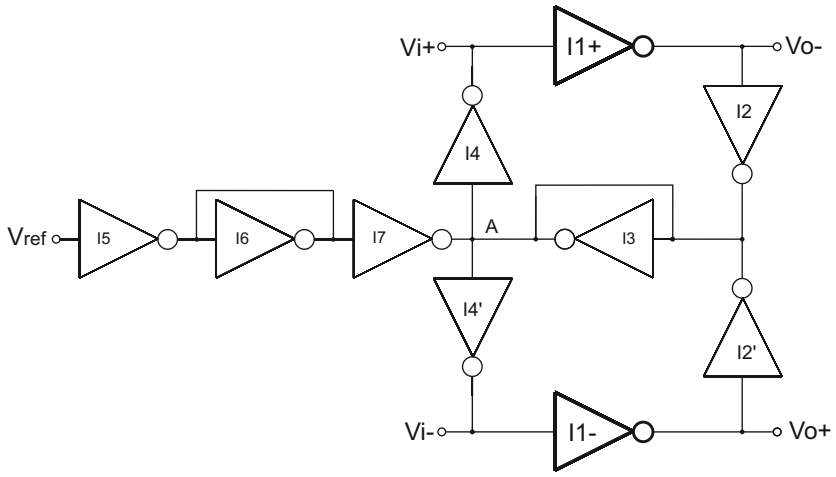

Figure 4.6. Schematic of a single pseudo-differential amplifier stage with CMFB.

phase. As aforementioned in short channel length technologies, the intrinsic voltage gain of transistors, given by $G_m r_0$ product, is quite low. Thus the operational amplifier must have more than one stage. A pseudo-differential amplifier provides the same gain for both the differential signal and the common-mode component. A CMFB loop and a Common Mode Feed Forward (CMFF) are therefore required to lower the common-mode gain and increase the CMRR. Moreover, to ensure the stability also for the common-mode loop, the common-mode gain has to be lower than 1, or still better an inverting gain is required. Thus avoiding to close the opamp in positive feedback for the common mode. That can be achieved by using an odd number of inverting stages, thus, a three-stage opamp architecture has been chosen. This choice makes more complicated the compensation network, that is performed with the reverse nested Miller technique [110]. Figure 4.7 shows the CMFF circuit. The CMFF provides a common mode gain of:

$$Voc = \frac{2gm_2}{gm_1} A_3 \tag{4.1}$$

where gm_1 and gm_2 represents the transconductance gain of inverters I1 and I2 (I2'), and A_3 is the voltage gain of inverter I3 (I3'). Inverter I1 should have twice transconductance gain with respect to inverter I2 (I2') in order to obtain $-v_{cm}$ at the input of inverter I3 (I3'). In order to suppress the common mode gain, inverter I3 (I3') should have the same transconductance gain of the first inverter of the pseudo-differential amplifier.

Figure 4.6 shows a single stage of the pseudo-differential amplifier with its common-mode loop. The inverters I2 and I2', whose outputs are connected together and to the inverter I3, connected in diode configuration, implement the common-mode estimator (CME). Inverters I5, I6 and I7 generate a reference signal related to the desired common-mode output voltage V_{ref}. This signal is compared with the

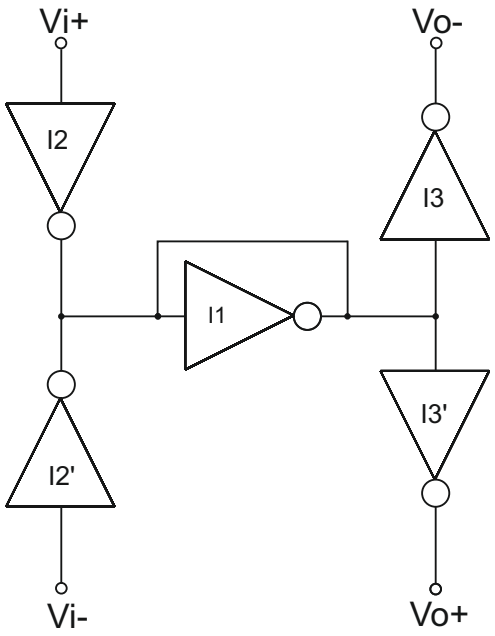

Figure 4.7. Inverter-based common mode feed forward

output of the CME in the current domain at node A, and the error signal is applied to inverters I4 and I4', whose outputs are connected to the inputs of the amplifier stage. The analysis of the circuit in figure 4.6, in case of a common-mode input $V_{i1} = V_{i2} = V_{ic}$, provides the output common-mode voltage:

$$V_{oc} = \frac{A_1 A_4 A_R v_{ref} - A_1 v_{ic}}{1 + A_1 A_2 A_4} \tag{4.2}$$

where A_1 is the voltage gain of I1, A_2 the gain of I2 loaded by the diode-connected I3, A_4 the gain of I4 (taking the effect of the source resistance into account) and A_R the voltage gain from v_{ref} to node A (considering also the loading effect of I3). Equation 4.2 shows that common-mode suppression depends on the gain $A_2 A_4$, and the v_{ref} path is able to impose the required dc voltage if $A_R = A_2$. This justifies the structure with the cascade of I5, I6 and I7: I7 has to be matched with I2, I5 is required to change the sign of the voltage gain, and the loading effect of the diode-connected I6 is needed to have $A_R = A_7 = A_2$. It has to be noted that standard CMFB configurations, where the control voltage from the CMFB controls a current generator, or varies the resistance of a triode-connected transistor, cannot be used, since there are no current generators in the proposed topology. Basically, I4 and I4' act as current sources, altering the equilibrium of currents at the input of the gain stage.

The complete scheme of the operational amplifier is shown in figure 4.8: CMFB loops are used on both the second and third stage, to reduce the common-mode gain

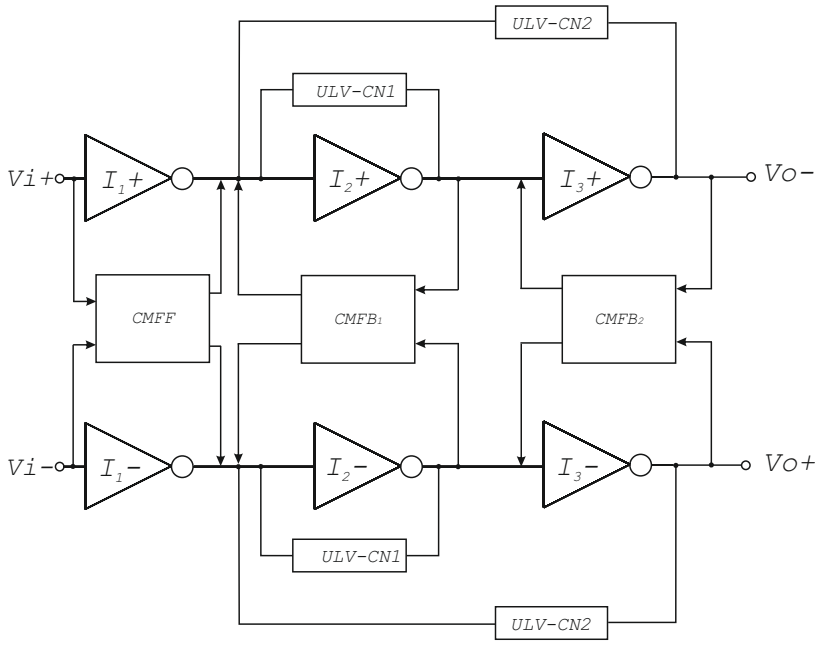

Figure 4.8. Schematic of the proposed inverter-based pseudo-differential amplifier.

and set the desired dc common-mode voltages; The three inverter stages are sized to optimize frequency behavior, and Ultra-Low-Voltage Nested Miller compensation network is used for stability.

4.0.2.1 Test Voltage Scalable OPA

The conversion frequency and resolution performance of a pipelined ADC are directly related to the opamp's behaviour. in a voltage scalable ADC the opamp must satisfy the ADC's requirement on the whole voltage range. The proposed amplifier wes simulated in STMicroelectronics 40nm CMOS technology. In order to reduce the minimum usable supply voltage, low-Vth MOS transistors have been used with 3 times the minimum gate length. The size of NMOS and PMOS devices in the inverter was chosen to set $V_o = V_{dd}/2$ when $V_{in} = V_{dd}/2$ is applied. The size of each inverter was scaled to satisfy the gain and bandwidth requirements and the design criteria for the CMFB. The amplifier was characterized with a capacitive load of 200fF, that is the same value of the sampling capacitors used in SHA.

The proposed structure of inverter based amplifier is able to operate at very low voltage values, in fact it can provide a gain of 20 dB with only 100 mV of voltage supply. Obliously at this voltage value the gain-bandwidth is only few kHz, but the total power dissipated is less than 500 pW. This allows to make this opamp suitable for very low voltage applications.

In figure 4.9 the variation of the performance of the opamp are repoted. The

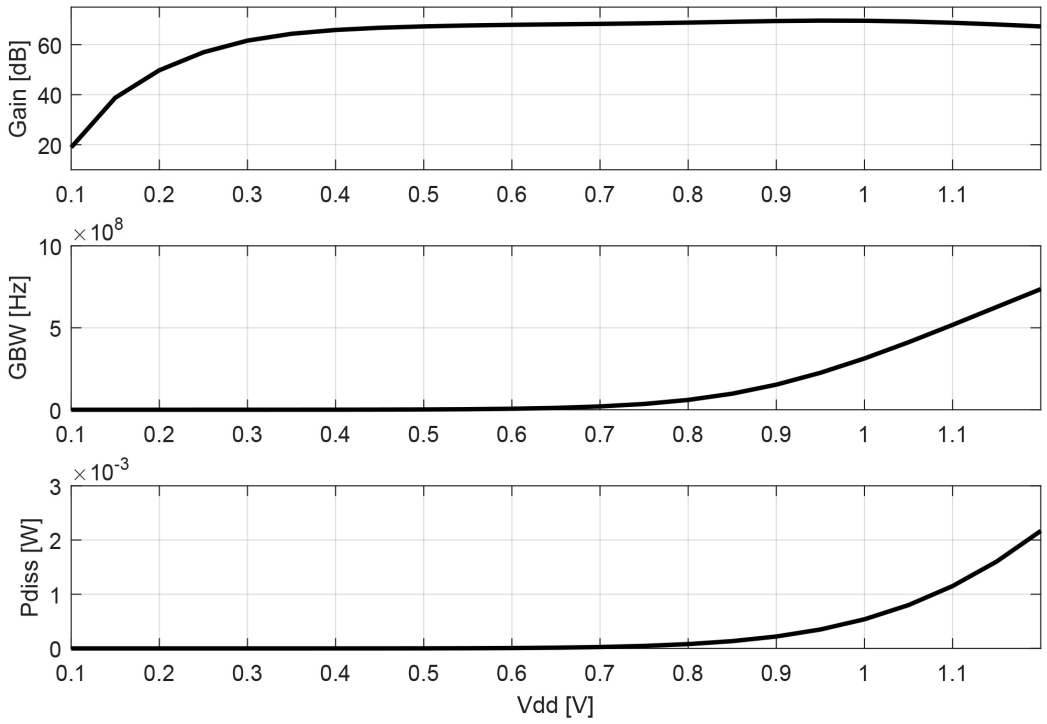

Figure 4.9. Voltage scalable opamp characterization

gain value is above 40 dB for voltage supply higher than 150mV, the gain-bandwidth product increases quadratically with the voltage supply as the power consumption.

In Table 4.3, the characterization results of proposed amplifier are shown. Differential gain remains approximatively constant for supply voltages as low as 0.5V, and an acceptable gain is still obtained for Vdd=0.3V, where the devices are biased in deep subthreshold. As expected, the unity-gain frequency f_u decreases with the supply voltage: as a consequence the settling time of the SHA will increase, resulting in a decrease of the maximum sampling frequency. As displayed in Fig. 4, the power consumption decreases quadratically with supply voltage, and drops below 1 μW when the supply voltage is under 0.4V. However the open loop gain remains above 63dB for a wide range of Vdd_L values. This keeps the gain error under a value that allows to use this amplifier in a 10-bit-ENOB ADC.

For an industrial point of view it is crucial that the circuit maintains its performance when temperature or process variation happens.

Figurs 4.10, 4.11, 4.12, 4.13 show the effect of tempreature variation on the DC-gain, gain-bandwidth product, phase margin and power consumption for different values of voltage supply. The curves in this figure are almost constant, thus, from this parametric analysis it can be concluded that the temperature variation has no negative impact on the behaviour of the opamp. Table 4.4 summarizes the effects of the process variation on the opamp's charateristics with a supply voltage of 1.2V,

Vdd [V]	Gain [dB]	Fu [MHz]	Pdiss[mW]
0.2	44.32	0.024	0.004
0.3	57.2	0.116	0.049
0.4	63.65	0.512	0.39
0.5	65.55	2.14	2.33
0.6	66.26	7.96	10.2
0.7	66.65	26.3	33.3
0.8	67.16	74.5	88.4
0.9	67.80	176	209
1	67.96	341	470
1.1	67.20	551	979
1.2	65.73	770	1837

Table 4.3. OPA open loop characterization

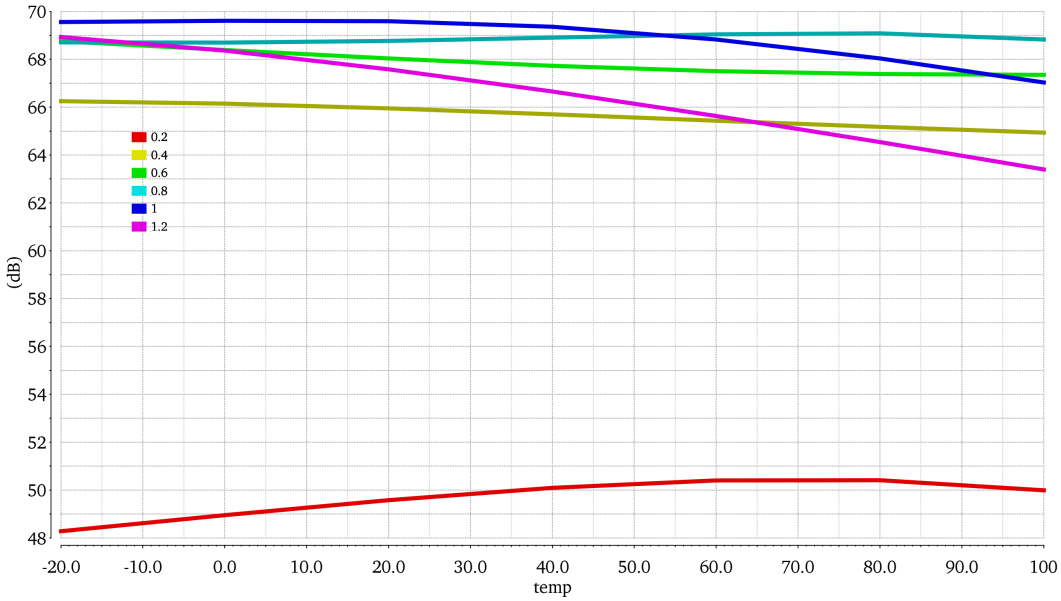

Figure 4.10. Temperature parametric analysis of gain behaviour vs voltage supply.

and from these results we can conclude that also the process variations do not affect dramatically the opamp's performance.

A 1000 points Monte Carlo analysis also highlights the robustness of the design respect to the process variations. In figures 4.14, 4.15, 4.16 and 4.17 the distributions of gain, gain-bandwidth product, phase margin and power consumption are reported when a voltage supply of 0.2V is applied. The Monte Carlo analysis results show that also when process variations occour, the performance of the opamp does not show a greath degradation that makes the opamp unusable. Taking as example

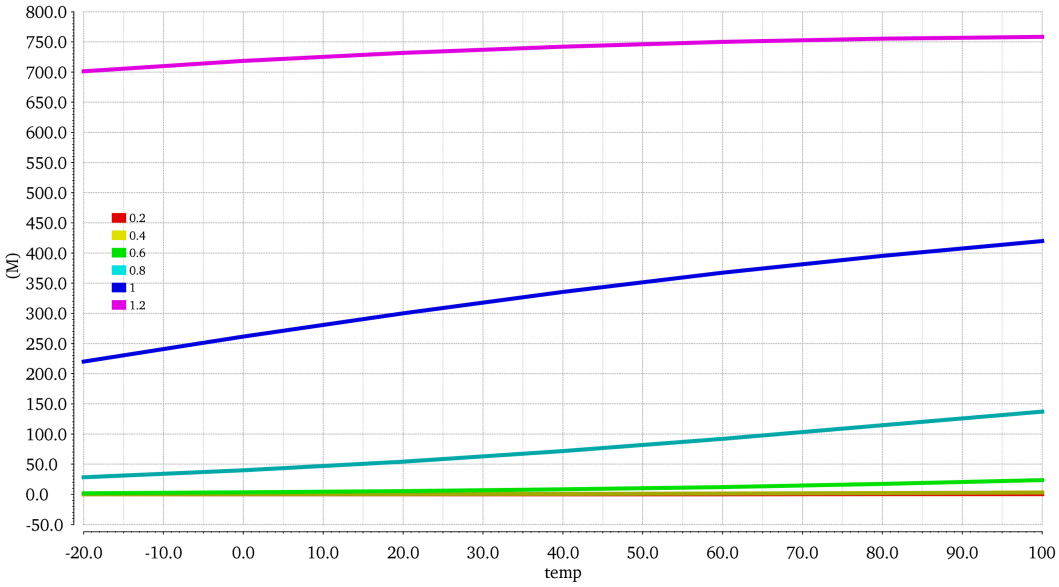

Figure 4.11. Temperature parametric analysis of gain-bandwidth product vs voltage supply.

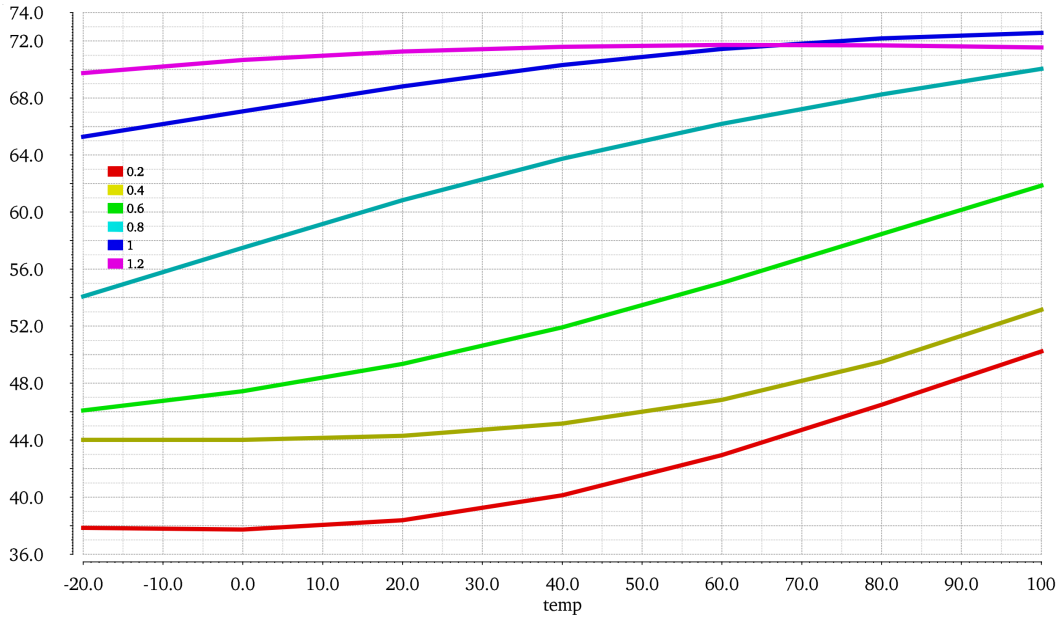

Figure 4.12. Temperature parametric analysis of phase margin vs voltage supply.

the distribution of the gain the Monte Carlo analysis shows a mean value of 47dB with a standard deviation of 9dB over 1000 samples, respect to 44dB of the nominal case. Also if the gain-bandwidth is considered, against 24kHz of the nominal case, the Monte Carlo analysis produces a mean of 20.7kHz with a standard deviation of 7.8kHz over 1000 points. Finally also the phase margin and the power consumption means of the Monte Carlo analysis are very close to the results of the nominal case.

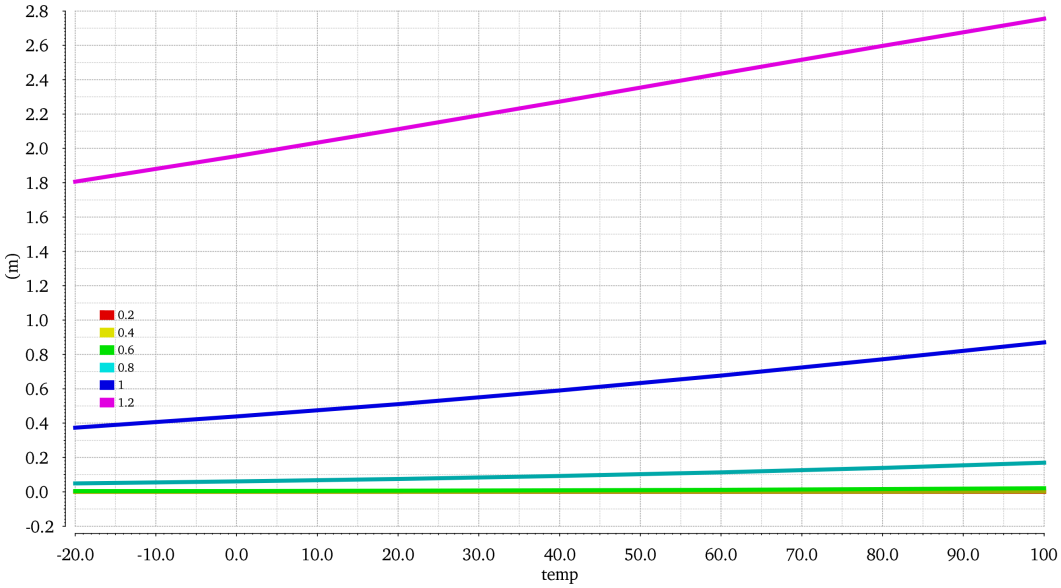

Figure 4.13. Temperature parametric analysis of power consumption vs voltage supply.

Corner	TT	FF	FS	SF	SS
Gain [dB]	65.7	67.7	56.8	57.7	67.7
Fu [MHz]	770	912	741	747	625
Phase Margin [°]	83.1	82.6	78.9	81.2	83.5
Pdiss [mW]	1.8	2.4	3	2.9	1.2

Table 4.4. OPA open loop characterization corner

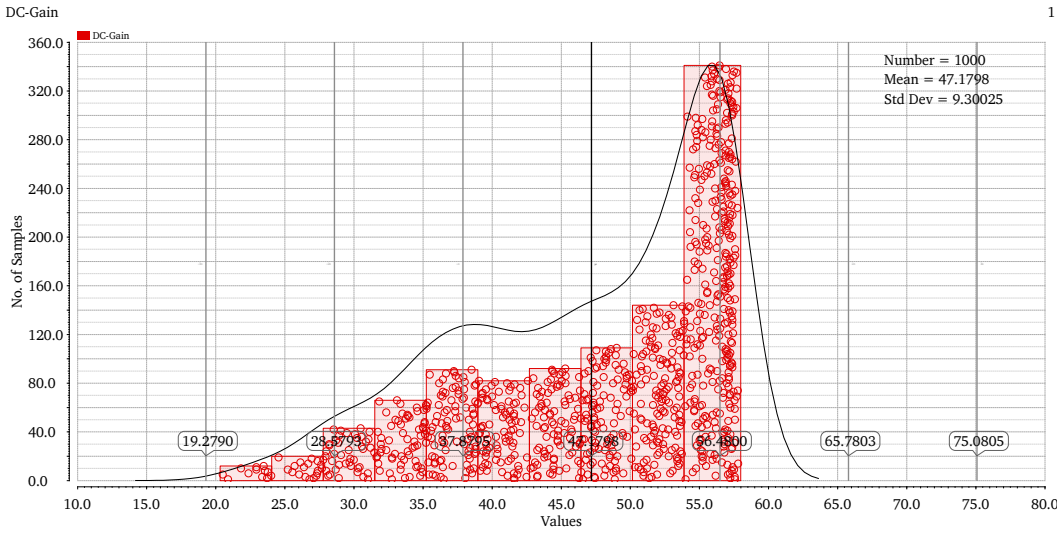

Figure 4.14. Effect of process variation on DC-gain when Vdd=0.2V is applied

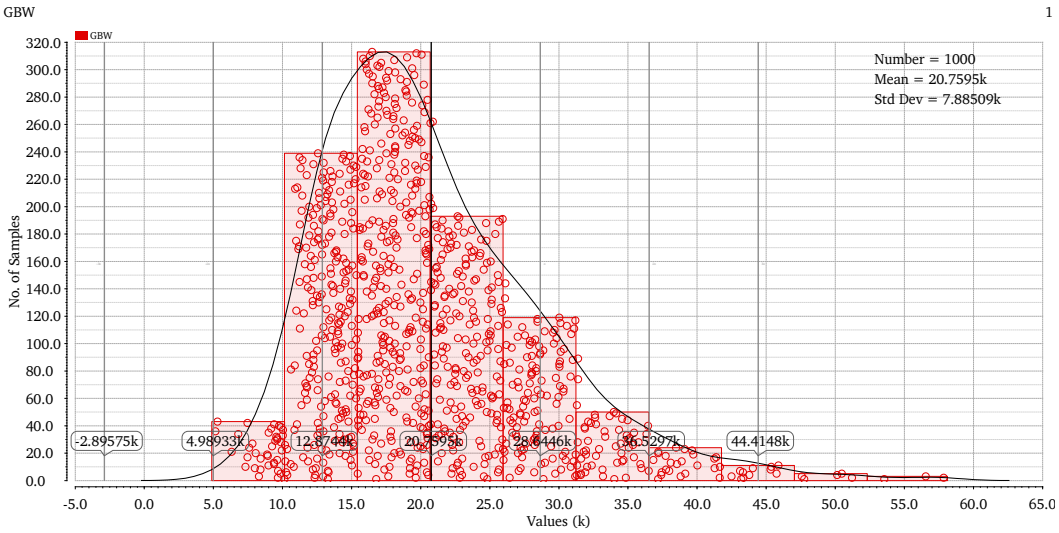

Figure 4.15. Effect of process variation on Gain-Bandwidth product when Vdd=0.2V is applied

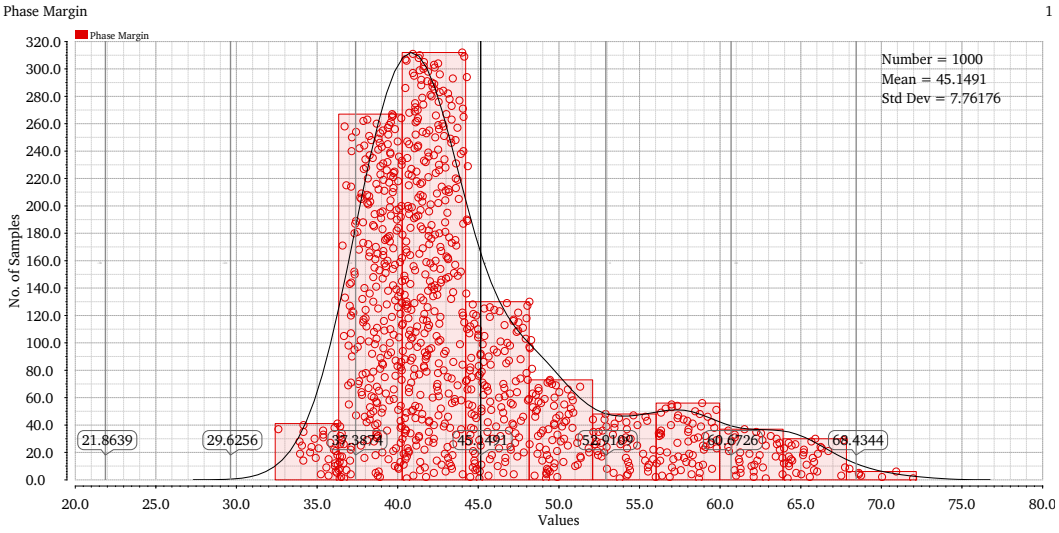

Figure 4.16. Effect of process variation on phase margin product when Vdd=0.2V is applied

Much better results in terms of standard deviation around the mean values are achieved for higher values of supply voltage. In fact as shown in figures 4.18, 4.19, 4.20 and 4.21 the didributions of the actual values has less spread compared to those obtained with lower supply voltages. Taking as example the standard deviation of the gain distribution (figure 4.18) due to the process variations is only 830mdB around a mean value of 66.8dB is clarely more concentrated than the distribution shown in figure 4.14 where a standard deviation of 9dB over 47dB of mean is achieved. Also the gain bandwidth product and the phase margin show a much narrower

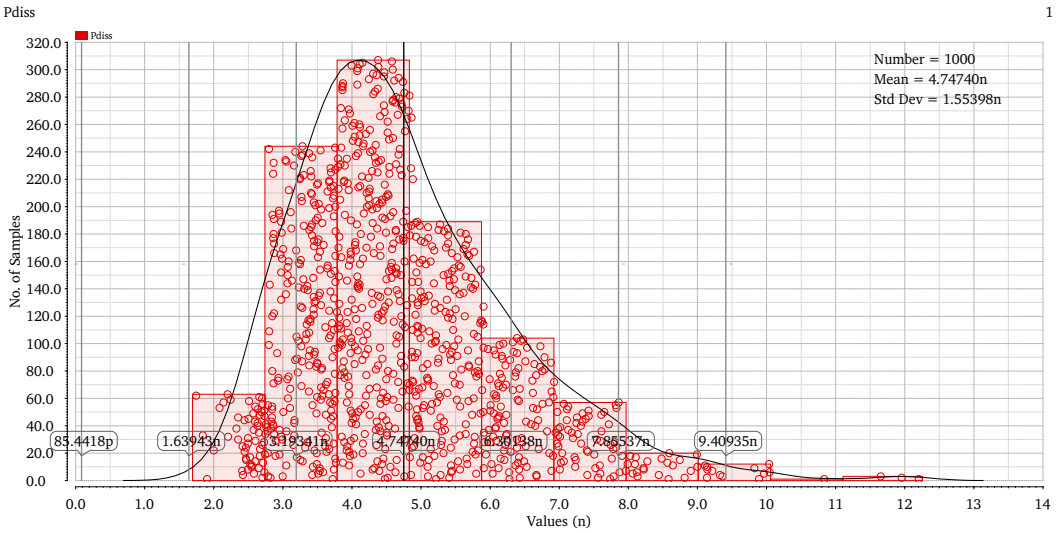

Figure 4.17. Effect of process variation on power consumption when Vdd=0.2V is applied

distributions. The results of the Monte Carlo Analysis are summarized in table 4.5.

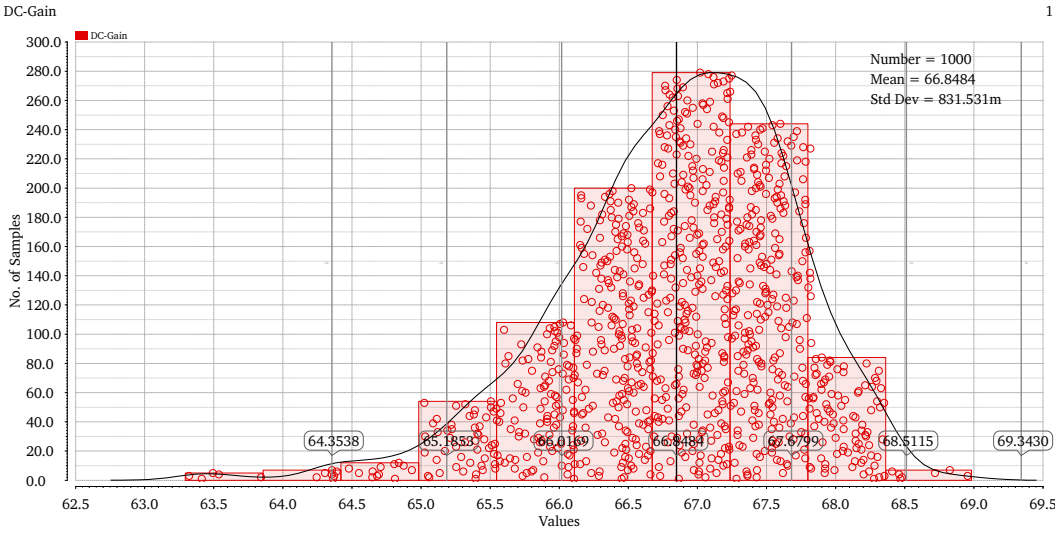

Figure 4.18. Effect of process variation on the DC-gain when Vdd=1.2V is applied

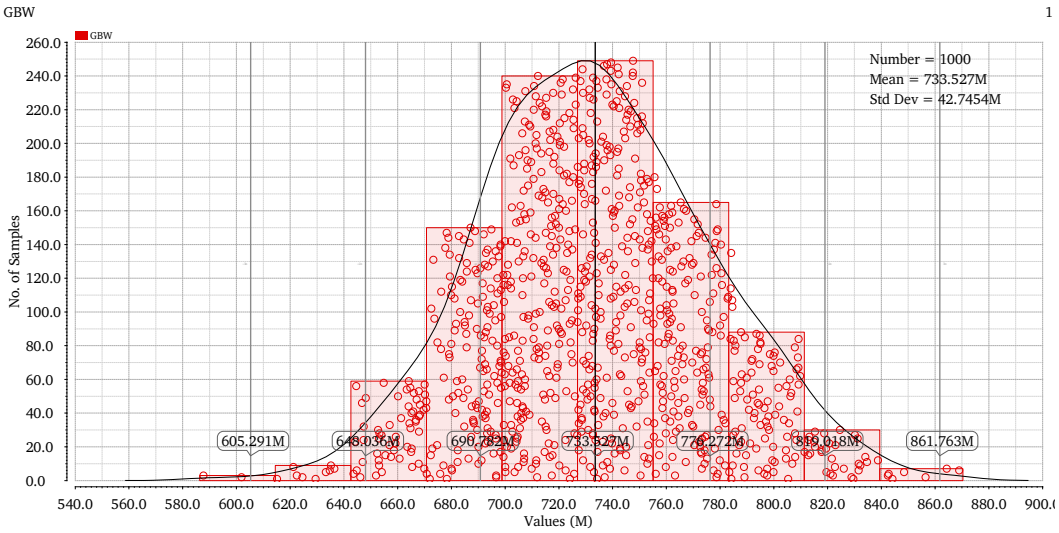

Figure 4.19. Effect of process variation on gain-bandwidth product when Vdd=1.2V is applied

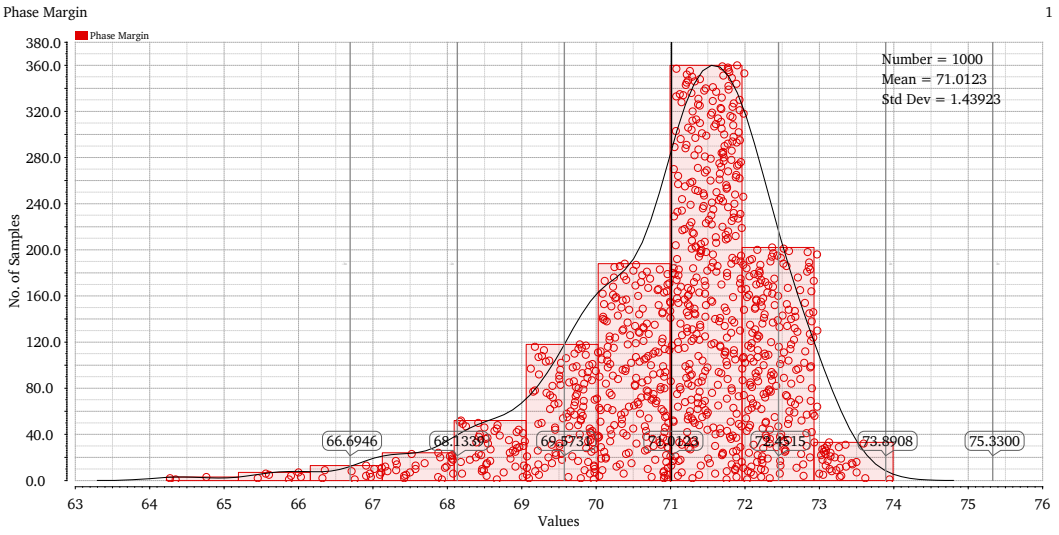

Figure 4.20. Effect of process variation on the phase margin when Vdd=1.2V is applied

4.0.3 Voltage Scalable Sample-and-Hold

The voltage scalable opamp was used to develop the two macro-blocks that compose the pipeline ADC and its front-end: the Sample-and-Hold and the MDAC.

The implemented Sample-and-Hold (figure 4.22) is based on the flip-around structure that can be easily modified in a Sample-and-Hold with gain as required for an MDAC. Moreover the Sample-and-Hold makes use of correlated double sampling (CDS) technique, to reduce the effect of offset voltage and flicker noise. In Switched-Capacitor circuits a critical role is played by the switches, whose resistance should be low and constant across all the input voltage range. This could be difficult to

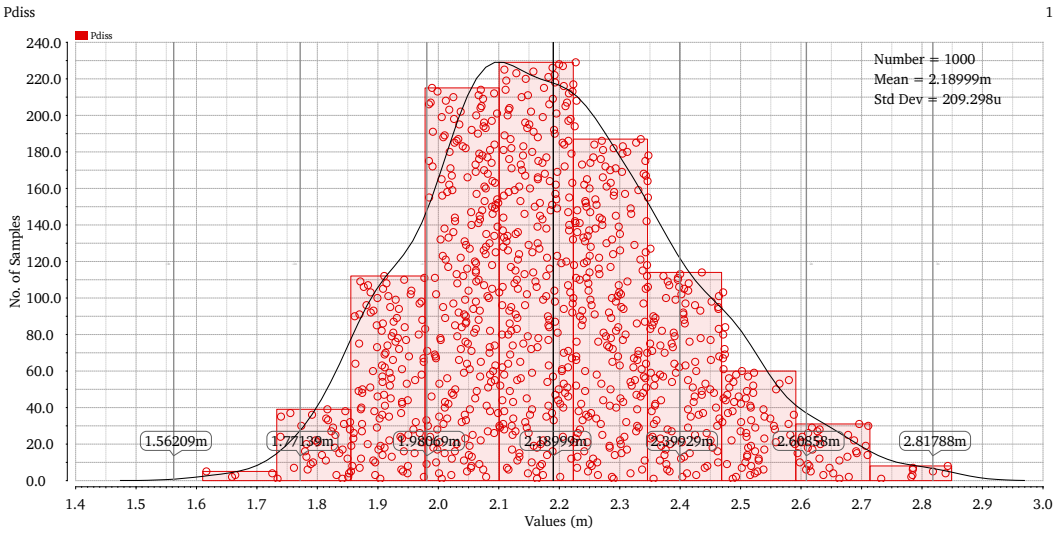

Figure 4.21. Effect of process variation on the power consumption when Vdd=1.2V is applied

Voltage supply [V]	0.2	1.2
Gain [dB]	47.2±9.3	66.8±0.8
GBW [Hz]	20.7±7.8 k	733± 42.7 M
$m\phi$ [°]	45.14±7.7	71± 1.43
P_{diss} [W]	4.74± 1.55 n	2.18± 0.2 μ

Table 4.5. Monte Carlo analysis summary

achieve in case of very low supply voltages, different solutions have been tested. Transmission gates have been used as switches in all cases, and different choices have been tried for the clock signal, exploiting the two different voltage domains that the system makes available: the system supply voltage (Vdd_S), that is the supply voltage of the overall ADC system, and the local supply voltage (Vdd_L), the supply voltage used for the opamps, that is derived from the former and is scaled according to sample frequency. Tested solutions are:

- Clock signal switching between 0 and Vdd_L. The amplitude of the clock scales down with the supply voltage of the amplifier. This allows a very low power consumption but in case of very low supply voltages it provides a switch resistance that is very high and sensitive to input signal level, since the V_{gs} of both transistors could result below the threshold voltage.

- Clock signal switching between 0 and Vdd_S. This solution allows maintaining a low switch resistance when amplifier supply voltage is scaled down. However two separate supply voltage domains are used in the SHA, and this complicates

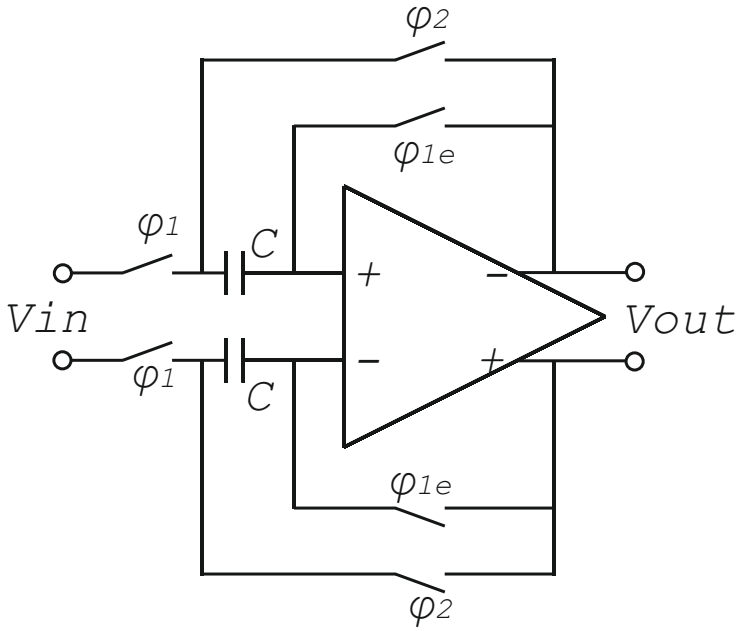

Figure 4.22. Flip-aroun Sample-and-Hold amplifier.

the layout of the circuit.

- Clock signal switching between 0 and $2Vdd_L$. To improve the performance of the switches at low supply voltage without using the system supply voltage, a voltage doubler can be used together with a clock signal switching between 0 and Vdd_L. However this complicates the layout if a single voltage doubler is used for each amplifier (or for the full ADC), and results in a low efficiency if each switch uses a local voltage doubler.

Simulations have been performed for the three solutions, and the use of two voltage domains (Sol.2) has been selected as the preferred solution, since it provides the best overall performance.

4.0.3.1 Test Voltage Scalable Sample-and-Hold

According to the obtained values of bandwidth, gain and phase margin, a voltage-scalable Sample-and-Hold circuit was simulated and characterized for different values of supply voltage and sampling frequency. In Figure 4.23, the differential output voltage of the SHA with a Vdd_L of 1.2V is displayed. In this case the rising, and falling times are 181ps and 268ps respectively, the slew rate value for the rising edge is 2.37GV/s and 981MV/s for the falling edge. In Table 4.6 the THD (Total Harmonic Distortion) values obtained at different voltages and sample frequencies are reported for an input differential amplitude of $0.9 * Vdd_L$ peak-to-peak. The table shows the effect of incomplete settling for a fixed value of supply voltage, and

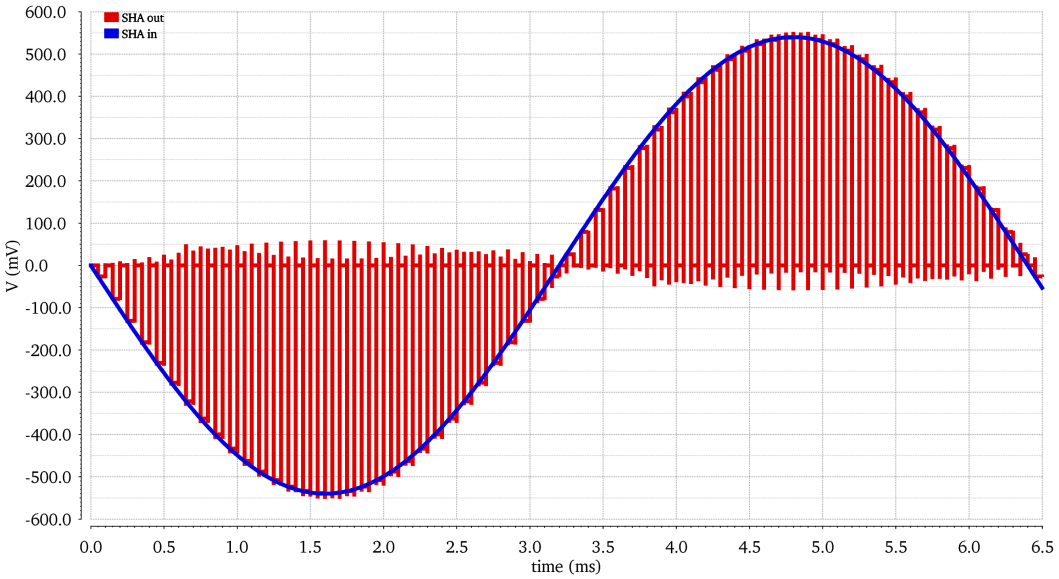

Figure 4.23

the effect of voltage scaling at fixed sample time. The maximum value of THD is reached for Vdd = 0.8V and sampling frequency 100 kHz, and corresponds to a maximum precision of 16 bit. As shown in Table 4.6, the proposed SHA can reach good performance even for very low voltage supply, obviously the minimum sampling time increases for low voltage supply, hence we can think to reduce dynamically the Vdd_L when the sample frequency requirement decreases.

4.0.4 Voltage Scalable Multiplying-DAC

An 1.5 bit MDAC is composed by a sub-ADC, a sub-DAC and a Sample-and-Hold with x2 gain as described previously, in this subsection the single blocks and the whole MDAC stage are described and characterized. The reconfigurable Sample-and-Hold can be used as a base to develop a x2 gain Sample-and-Hold, that is required to implement the 1.5 bit MDAC structure.

As shown in figure 4.24, by splitting the sampling capacitor in two, and adding a digital input path, a x2-Sample-and-Hold-Amplifier (SHAx2) structure can be easily obtained. The $\pm D$ input allows to add the result of the sub-conversion with the input signal, and thus obtain as output the quantization error of the sub-converter. Setting the gain exactly equal to 2 is needed to scale the quantization error equal to the maximum dynamic input of the next stage, and overcome saturation. The SHAx2 uses the inverter-based opamp previously developed for the Sample-and-Hold. The phase margin and the settling response can be slightly different in SHAx2 stage because the reaction ratio is doubled respect to the Sample-and-Hold. About the switches, the same consideration made for the Sample-and-Hold block can be done.

Fs [ns] Vdd[V]	0.4 V	0.6 V	0.8 V	1 V	1.2 V
10	-	-	33.6	68	70.7
15	-	-	33.6	69.4	74.5
20	-	-	33.6	78.5	76.7
50	-	-	61	76.6	78.5
70	-	-	71.5	76.6	78.7
170	-	-	89.7	76.5	78.9
350	-	37.6	90.42	76.6	78.9
2000	-	85.7	92.4	76.7	79.1
10000	42.3	73.9	100.9	77.1	79.6

Table 4.6. THD for different values of Vdd and sampling period

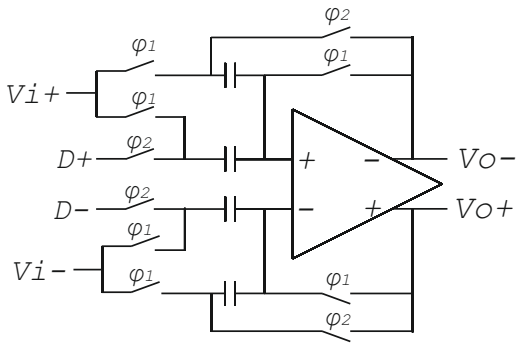

Figure 4.24. Sample-and-Hold with 2X gain

Thus, for the same reasons esposed for the Sample-and-Hold, transmission gate structure was chosen to implement the switches, and the driving signals are the same of the Sample-and-Hold. An important element in the MDAC is the comparator, and a number of considerations can be made for its requirements. The comparator is the second source of power consumption in a MDAC stage, then some consideration on the energy efficiency is needed to optimize the FOM of the ADC. In literature static and dynamic structures of comparator are available. The simplest static comparator is substantially a two stages OTA, but without the compensation network. Thus the energy efficiency is almost the same of a class-A amplifier that is too low to be used in low power ADC, thus, a comparator structure that guarantees lower power consumption is preferable. For this purpose a dynamic comparator represents a valid trade-off between linearity and power consumption. In fact it is substantially a latch, based on differential pair and regenerative loop. In a dynamic comparator there is no static power consumption, and its power consumption is related to the clock frequency as in CMOS logic gates. This dependence allows a reduction of the power consumption by a suitable clock frequency scaling as described in previous

chapter.

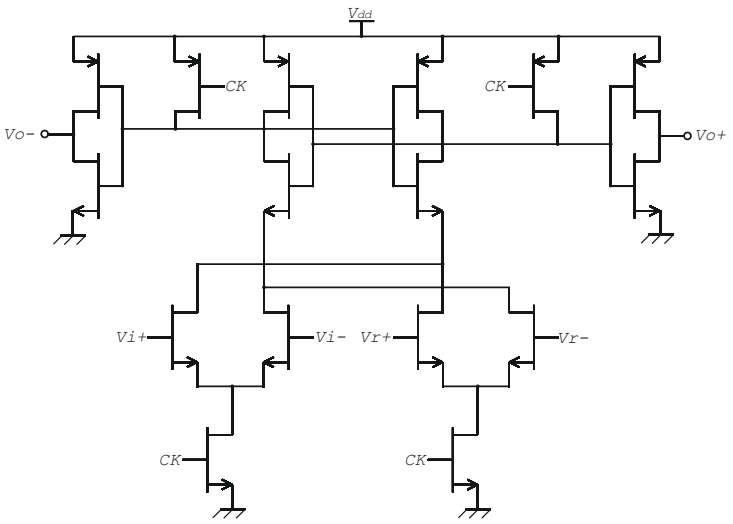

Figure 4.25. Dynamic comparator

The dynamic comparator schematic is shown in figure 4.25. The clock signal controls both the differential pair and the output buffer. When the clock signal is low the differential pairs are disabled and both the output are reset. When the clock signal is high the differential pairs are enabled, and control the regenerative loop above them. The behaviour of the comparator is shown in figure 4.26 where single ended signals are reported. The green trace of the figure is the analog input signal, the purple line is the reference voltage and the orange line is the output. Note that the output is reset by the clock signal that is not shown in the figure.

The sub-ADC involved in the MDAC is composed by a couple of dynamic comparators with crossed reference voltages, as shown in figure 4.27, its output signals controls a 3-to-1 differential multiplexer that realizes the sub-DAC funcion.

The relation between clock frequency and power consumption of a single comparator is shown in figure 4.28. As expected the mean power consumption increases almost linearly from 70nW at 200 kHz to 30μW at 200 MHz.

4.0.4.1 Test Voltage Scalable Multiplying-DAC

Assembling togheter all the single blocks the complete MDAC stage can be obtained, as reported in figure 4.29. In figure 4.29 the Logic block takes as input the output signals of the comparators and produce as output the 1.5 bit of partial results of the conversion, it also generates the control signal for the sub-ADC. The capacitors of the SHAx2 block are set equal to 50fF because is a trade off between mismatch, noise and speed. The power supply is split in two for the digital and the analog parts. The digital control logic, the dynamic comparators and the switches are connected to a Vdd_S constant voltage supply equal to 1.2V. The SHAx2 block

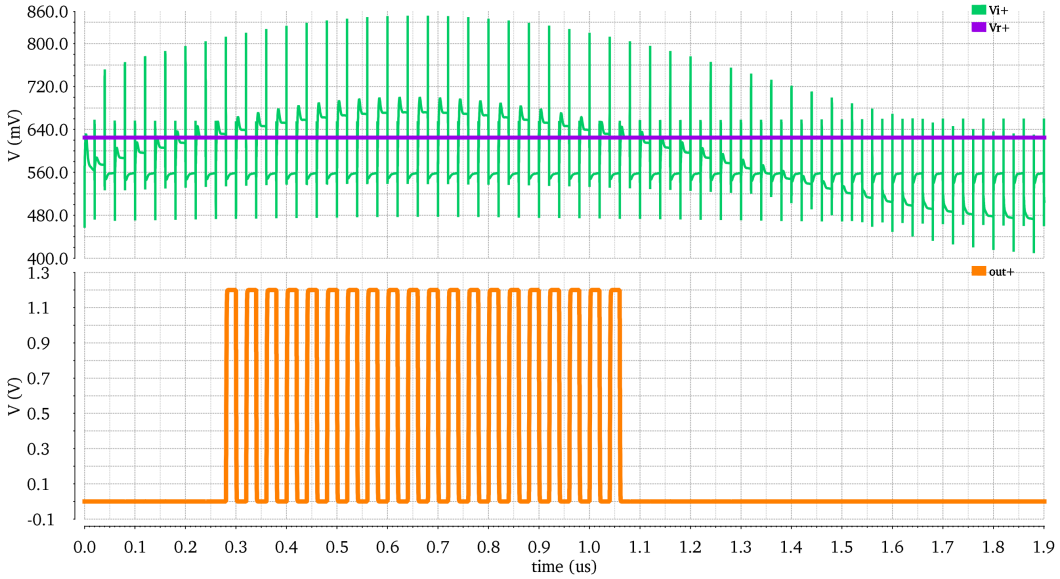

Figure 4.26. Dynamic comparator transient analysis

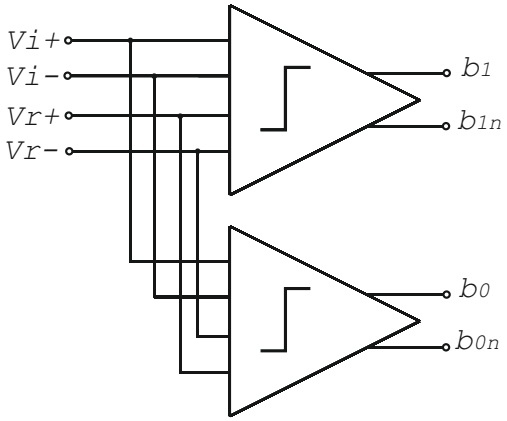

Figure 4.27. sub-ADC implementation

istead is connected to a variable voltage supply Vdd_L that can assume values in the range from 0.3V to 1.2V. The input signal of the chain is parametrized respet to the variable voltage supply, and is set to Vdd_L peak-to-peak differential. The MDAC stage as the Sample-and-Hold was caracterized for different values of Vdd_L. To obtain results of realistic case the test bench is composed by an inverter-based voltage-scalable Sample-and-Hold that feeds a chain of two MDAC stages, the results reported below are related to the first MDAC of the chain. Thus, as shown in figure 4.30 the signal at the input of the MDAC is not an ideal single spectral line, but is a realistic sampled signal. At the output of the first stage the analog residue signal is added to the digital signal to evaluate the distortion introducted by the MDAC (i.e. an ideal backend ADC is assumed).

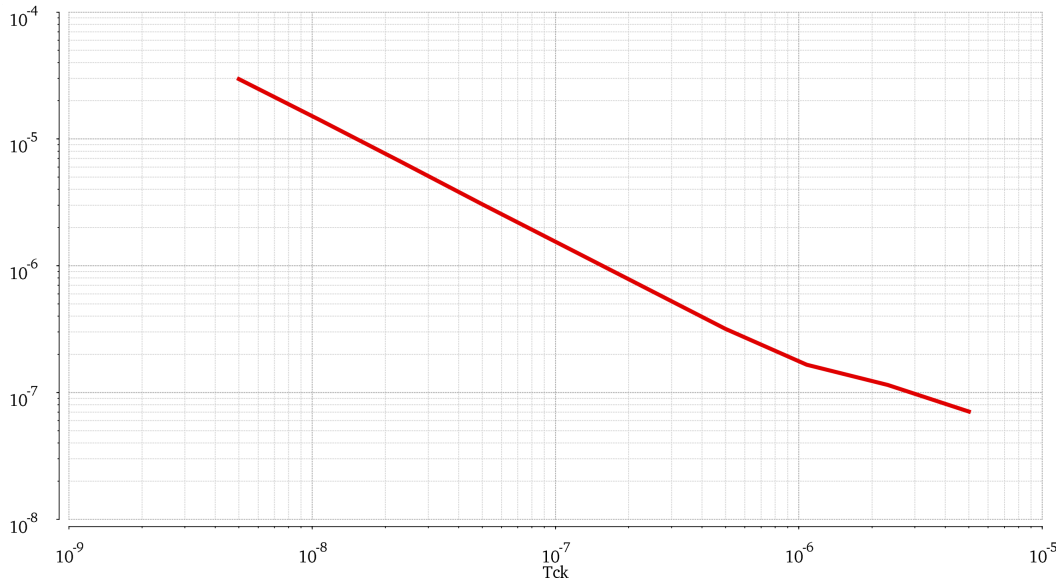

Figure 4.28. Power consumption VS Clock period

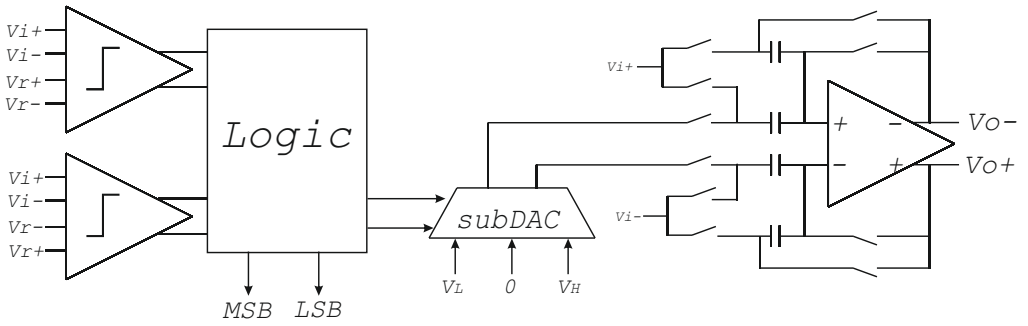

Figure 4.29. 1.5 bit MDAC stage implementation

The effect of the voltage scaling impacts on the phase margin of the opamp, that depends also on the amplitude of the input signal. For this reason at lower supply voltages the maximum amplitude of the signal must be reduced, or the compensation network must be tuned to guarantee the stability of the system. In table 4.7 are reported the results of the MDAC, and for an easy evaluation of the effect of the MDAC on the signal linearity also the results of the Sample-and-Hold are reported.

For each voltage value in table 4.7 were chosen the minimum sampling time that allows to obtain 10 bit of ENOB. For the first four rows the amplitude of the signal is set to $\frac{1}{4}Vdd$, but, when the supply voltage is reduced to 0.6V or less, the phase margin is reduced when high amplitude signal is applied because the phase margin of a class-AB depends by the amplitude of the signal. Halving the ratio between the power supply and and the input signal this issue is solved. As result from the table 4.7, for very low voltage supply also the linearity of the Sample-and-Hold is worsed,

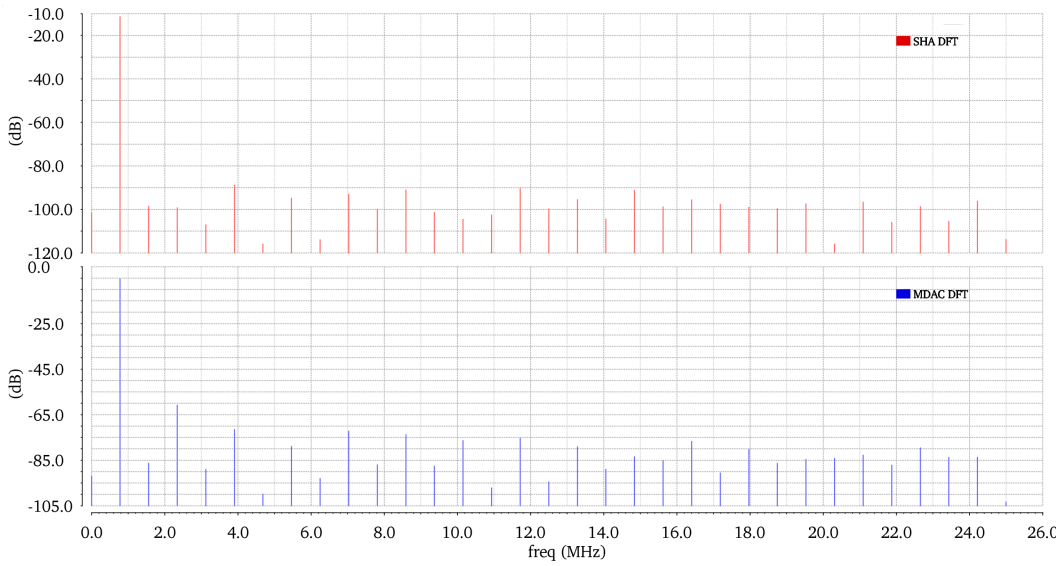

Figure 4.30. comparison between the DFT of the output signal of the Sample-and-Hold, and the recostructed signal at the output of the first MDAC.

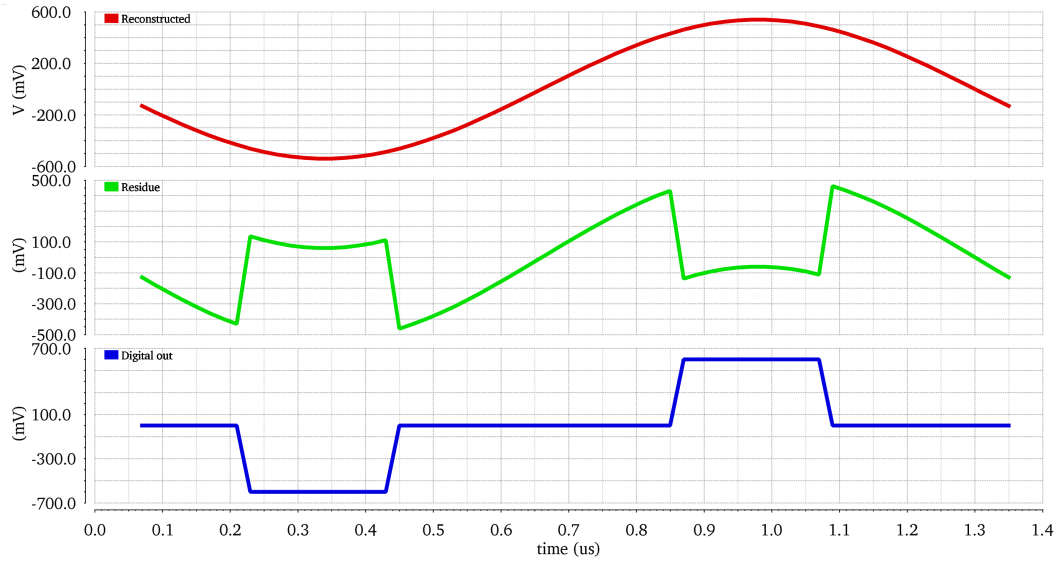

Figure 4.31. Reconstruction of the signal at the output of MDAC stage.

thus the output of the MDAC can not reach 10 bit of ENOB for supply voltages less than 0.5V. The table 4.7 gives also the relation between sampling frequency and supply voltage.

4.0.5 Voltage Scalable Pipeline ADC

The voltage scalable Sample and Hold and the voltage scalable MDAC are used as building blocks to implement a nominal 12-bits voltage scalable ADC pipeline.

Vdd [V]	Tck	THD_{SHA}[dB]	$ENOB_{SHA}$	THD_{MDAC} [dB]	$ENOB_{MDAC}$
1.2	15 ns	70.15	11.94	71.9	11.59
1	50 ns	65.8	11	64.3	10.4
0.8	120 ns	73.9	12.56	65.22	10.54
0.6	800 ns	68.3	11.6	36.20	5.72
0.6	800 ns	92.15	15.59	67.86	10.98
0.5	1.5 μs	62.1	10.6	58.9	9.5
0.4	6 μs	57.5	9.8	50.60	8.11
0.3	16 μs	38.7	6.73	34.9	5.5

Table 4.7. MDAC and Sample-and-Hold characterization for different voltage supply

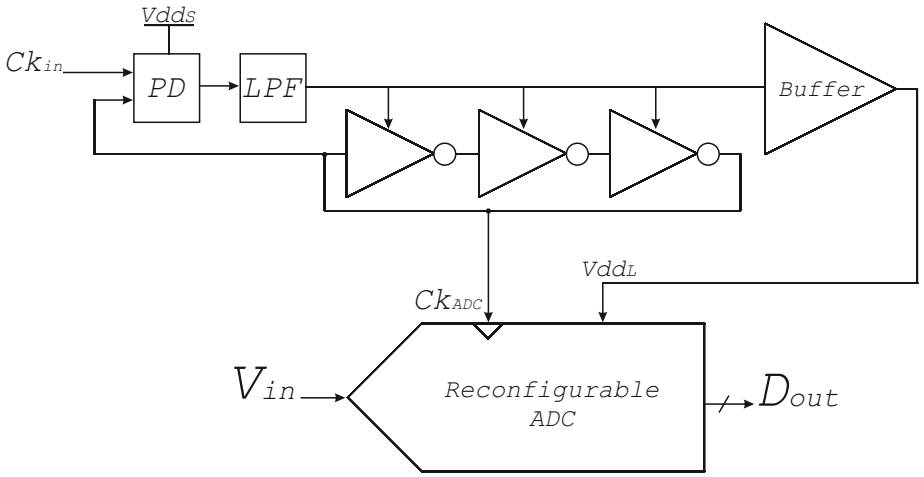

Figure 4.32. Clock control loop

The clock input is used to set automatically the local voltage to the lower value required to overcome settling error. This feature can be made easily through a lookup table (LUT) whit couoples of voltage-frequency data stored inside it. To enable this function additional analog and digital circuits are required to measure the input clock and read the data from the LUT, and however the number of allowed input frequencies are limited to the size of the LUT. A different solution that overcome this limitation is due to an automatic clock control loop that exploit the relation between the value of the voltage supply Vdd_L and the oscillation frequency f_{osc} of a ring oscillator. If the Inverters of the ring oscillator are sized as the inverters involved in the pseudo-differential inverter-based OTA, the oscillation frequency of the ring oscillator follows the same trend of the opamp's f_0 when the applied voltage has been changed. The schematic of the automatic clock control loop is shown in figure 4.32.

The reconfigurable pipeline ADC is composed by the voltage-scalable Sample-and-Hold followed by 11 voltage-scalable MDAC stages. No digital correction is implemented in order to have direct access to the raw conversion signals that can be used by the Volterra based calibrator proposed in [65] discussed in chapter 3. In the first implementation no opamp or capacitor sharing techniques were applied because the SHAX2 steges uses the CDS technique to limit the offset of the opamp, but in future development opamp sharing technique might be used to achieve a significative improvement of the energy efficiency.

4.0.5.1 Test Voltage Scalable Pipeline ADC

The testbench used to characterize the single MDAC stage was used as base to test the performances of the whole pipeline chain. The digital signal was aligned and converted in analog domain through a MATLAB function to calculate the THD and the ENOB. Table 4.8 summarizes the performance results of the entire pipeline ADC. The ENOB achieved by the pipeline is almost constant in the range 0.4V to 1.2V.

Vdd [V]	Tck	THD_{SHA}[dB]	$ENOB_{SHA}$	THD_{Pipe} [dB]	$ENOB_{Pipe}$
1.2	15 ns	70.04	11.92	53.9	8.67
1	50 ns	64	11	54.3	8.86
0.8	120 ns	75.4	12.8	65.77	10.63
0.6	800 ns	95.6	16.17	65.3	10.55
0.4	6 μs	58.59	10	52.3	8.4

Table 4.8. Pipeline and Sample-and-Hold characterization for different voltage supply

Chapter 5

MDAC with low sensitivity to OPA's finite gain error

In pipeline ADCs the main limitation on the accuracy of the conversion is due to the mismatch between the capacitors, and the finite gain of the opamp. For low values of capacitors the capacitors mismatch of the early stages can be dominant, but for the latter stages is the gain error the principal error source. Thus, reducing the gain error is fundamental to obtain an high-resolution converter, because the gain error is linear on the single MDAC stage, but the architecture of the pipeline ADC converts it to a nonlinear error of the overall conversion, thus generating distortion. Different solutions are available in literature to limit the effects of finite gain error, but all of them exploit the canonical negative feedback loop. A negative feedback loop allows to improve linearity, noise performance and to set a precise gain. This is possible as long as the opamp is ideal and thus its DC-gain is infinite. Sadly, in a phisical world the gain of the opamp is not infinite thus also the improvement of the performance is finite, this means that gain error related to the gain of the opamp appears. In sub-micron technologies, as described in chapter 2, the design of high gain opamps is very challenging, and requires stacked or multi-stage structures. But in multistage structures heavy compensation network are required that lead to a dramatic reduction of the bandwidth. Also, in stacked structures the main limitation is on the dynamic of the signal, that makes them unsuitable for low voltage applications. A possible way to overcome the limitations of the classical feedback loop is to use a different feedback paradigm, that unlinks the relation between the open-loop gain of the opamp and the gain error of the structure. This is possible by an active feedback loop that is theoretically able to delete the gain error by forcing an exact relation between the open loop gain of two opamps. This avoids the need for digital calibration because it removes the error source. In the first half of this chapter the active feedback technique is introduced and the analytical rules to manage offset and frequency behaviour are provided. After that, a particular case of

switched capacitors application is introduced, and a 1.5bit MDAC stage is described. In the second half of the chapter, assumed a worst case scenario of deep-submicron application, where it is dificult to design high-gain and wide-band opamps, a current mirror based fully-differenial opamp topology is proposed to implement the active feedback loop. Finally, the results of a 10bit 50MS/s pipeline ADC simulated in CMOS 40nm STMicroelectronics technology are reported.

5.1 Active Feedback Structure Introduction

In a classical feedback structure the finite gain error can be reduced by increasing the open loop gain of opamp, but this error can never be equal to zero. Moreover in very short channel CMOS technologies achieving high gain becomes difficult, due to the reduction of the intrinsic gain of the devices, and the limited supply voltage prevents the use of cascode topologies. Therefore the effect of finite opamp gain becomes a non-negligible source of error. To overcome this limitation an active feedback structure was proposed in [111], that is able under opportune conditions to delete matematically the gain error of the opamp.

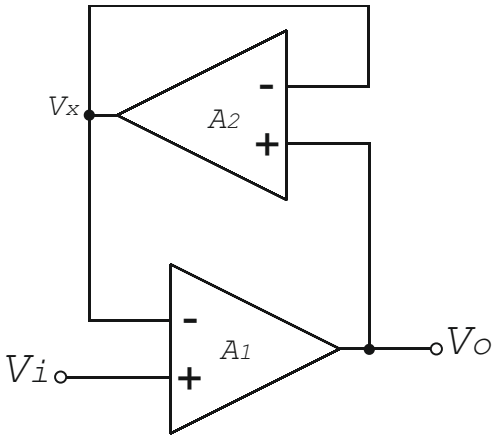

Figure 5.1. Active feedback scheme

Figure 5.1 shows the proposed architecture. In this structure a voltage buffer is used to close the feedback loop and cancel the gain error of the main amplifier. The tranfer function of the system in figure 5.1 is:

$$\frac{V_o}{V_i} = \frac{A_1(1+A_2)}{A_1A_2 + A_2 + 1} \tag{5.1}$$

The gain error is defined as difference between the ideal and actual gains

$$\epsilon_g = \left(\frac{Vo}{Vi}\right)_{ideal} - \left(\frac{Vo}{Vi}\right)_{real} = \frac{A_2 - A_1 + 1}{A_1A_2 + A_2 + 1} \tag{5.2}$$

thus chosing $A_1 = A_2 + 1$ the gain error can be nullified. Of course, this precise expression can be reached in nominal process corner, but PVT variations must be taken into account. Such a fine tuning, although accomplished through an automatic regulation section, will still be affected by a residual error due to unavoidable mismatches. This technique can be applied also to discrete-time circuits, such as Sample-and-Hold and MDAC structures [112]. In the next subsection classical and active-feedback-based structures for Sample-and-Hold and MDAC are considered, and an analytical evaluation of the gain error in such structures are provided.

5.1.1 Classical Feedback x2 Gain Sample-and-Hold Analysis

At first we consider the flip-around sample-and-hold circuit with x2 gain shown in figure 5.2

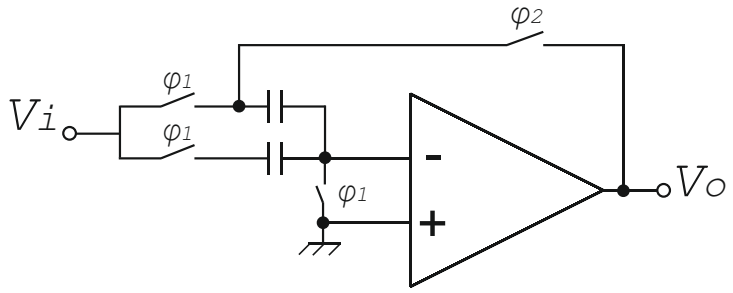

Figure 5.2. Flip-around Sample-and-Hold with x2 gain

The input-output transfer function can be calculated by exploiting the conservation of charge between sample (ϕ_1) and hold (ϕ_2) phases. The total charge in the circuit during the sample phase is due by

$$Q_{sample} = 2CV_i \tag{5.3}$$

also during the hold phase the total charge is

$$Q_{hold} = CV_0 \left(1 + \frac{1}{A_1}\right) + C\frac{1}{A_1} \tag{5.4}$$

where A_1 is the gain of the opamp, and C the sampling capacitance. Under the charge conservation hypothesis, we get

$$\frac{V_o}{V_{in}} = \frac{2A_1}{2 + A_1} \tag{5.5}$$

and the gain error is

$$err = 2 - \frac{2A_1}{2 + A_1} = \frac{4}{2 + A_1} \tag{5.6}$$

Eq.(5.6) shows that in classical feedback paradigm the gain error can be reduced to the desired value at the cost of increasing the gain value of the opamp. Increasing the gain means the employment of stacked amplifier structures or multistage amplifiers, that bring a reduction of the dynamic or an increase of the power consumption. Moreover, multistage amplifiers require complex compensation networks that reduce the bandwidth of the amplifier.

5.1.2 Active Feedback x2 Gain Sample-and-Hold Analysis

The active feedback concept can be extended also for discrete time circuits. Figure 5.3 shows the principle scheme of active feedback applied to a flip atound Sample-and-Hold with x2 gain.

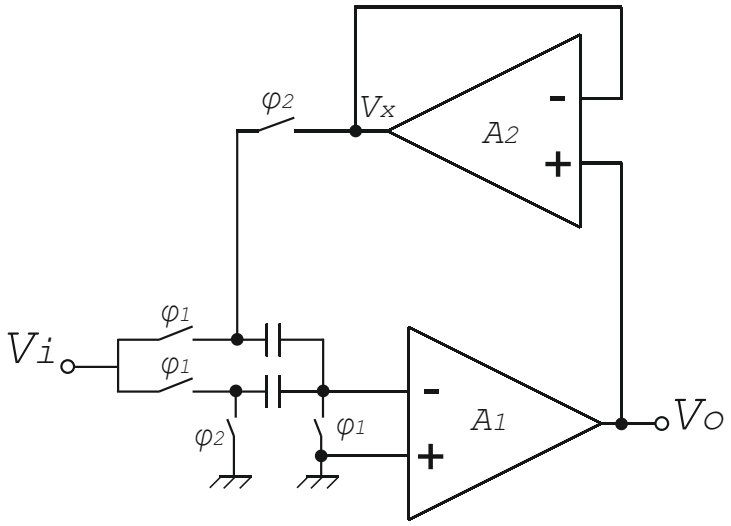

Figure 5.3. Active feedback applied to a Sample-and-Hold with x2 gain structure

During the sample phase the equivalent circuit is the same as the classical feedback structure, and the charge in this phase is $Q_{sample} = 2CV_i$. During the hold phase the equivalent circuit is different and the stored charge is

$$Q_{hold} = C\left(V_x + \frac{V_o}{A_1}\right) + C\frac{V_o}{A_1} \tag{5.7}$$

where $V_x = V_o\frac{A_2}{1+A_2}$ and A_2 is the gain of the opamp in the feedback path. Under the charge conservation hypothesis we get

$$\frac{V_o}{V_{in}} = \frac{2A_1}{2 + \frac{A_1A_2}{1+A_2}} = \frac{2A_1(1+A_2)}{2(1+A_2)A_1A_2} \tag{5.8}$$

and the gain error for this structure is

$$err = 2 - \frac{2A_1(1+A_2)}{2(1+A_2)A_1A_2} = \frac{2[2(1+A_2)-A_1]}{2(1+A_2)A_1A_2} \tag{5.9}$$

The numerator of (5.9) can be equal to zero if the ratio between the gains of the opamps is exactly $A_1 = 2(A_2 + 1)$. This means that the overall gain error in this structure can be mathematically cancelled. The crucial point is that the nulling of the gain error can be reached for very low-gain values, the precision in the ratio is the key point. This allows the use of simple opamp architectures where a small amount of power consumption is required, and no complex compensation techniques are involved. Furthermore, this architecture is very useful in nanometric technology nodes, where it is very challenging to reach high gain values.

5.1.3 Classical Feedback MDAC Analysis

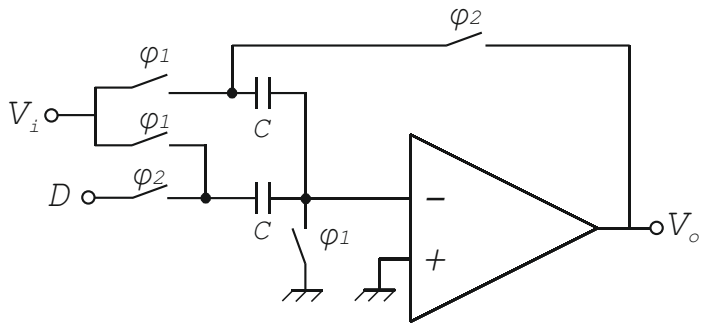

Figure 5.4. 1.5 bit MDAC schematic

Move from Sample-and-Hold to MDAC is quite simple. Now considering the schematic of the 1.5bit MDAC is shown in figure 5.4, during the sample phase the equivalent circuit is the same as the classical feedback structure, and the charge in this phase is $Q_{sample} = 2CV_i$.

During the hold phase the equivalent circuit is shown in figure 5.5 and the total charge is

$$Q_{hold} = CV_0\left(1 + \frac{1}{A_1}\right) + C\left(D + \frac{V_0}{A_1}\right) \tag{5.10}$$

By taking into account also the input capacitance C_{in} of the opamp, we get

$$V_0 = \frac{2V_i - DV_R}{1 + \frac{1}{A_1}\left(2 + \frac{C_{in}}{C}\right)} \tag{5.11}$$

where A_1 is the opamp gain and C the sampling capacitance. The input capacitance practically reduces the opamp gain to

$${A_1}^* = \frac{A_1}{1 + C_{in}/2C} \tag{5.12}$$

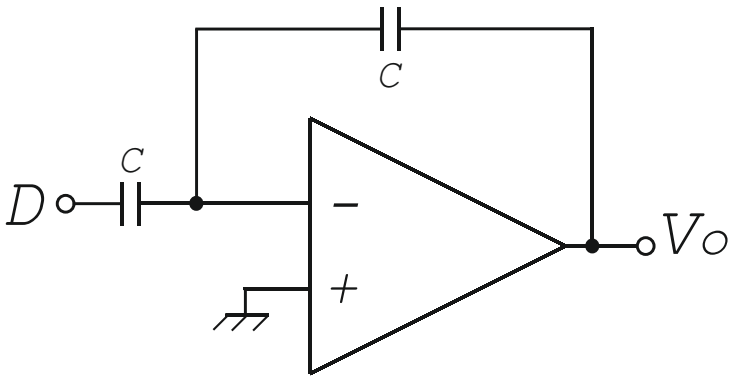

Figure 5.5. Single ended equivalent circuit of the MDAC in hold phase

and (5.11) can be written as:

$$V_0 = \frac{2V_i - DV_R}{1 + \frac{2}{{A_1}^*}} \tag{5.13}$$

Eq. (5.13) shows that the ideal transfer function of the MDAC: $V_0 = 2V_i - DV_R$ is asymptotically reached for ${A_1}^* \to \infty$. This condition can not be reached in a real circuit but it is possible to use an operational amplifier with high gain. On the other hand, high gain can be obtained with complex architectures or multi-stage opamps, that cause more power consumption, and require a compensation network that brings a limitation of the bandwidth.

5.1.4 Active Feedback MDAC Analysis

In figure , 5.6 a non inverting voltage follower is employed in the feedback loop.

Figure 5.7 shows the equivalent schematic during the hold phase.

In this case, the charge in the sample phase is still $Q_{sample} = 2CV_i$, but in the hold phase it becomes:

$$Q_{hold} = C(DV_R + V_o/A_1) + C(V_x + V_o/A_1) + C_{in}V_o/A_1 \tag{5.14}$$

where $V_x = V_o A_2/(A_2 + 1)$, and A_1 and A_2 are the open loop DC-gain of the main operational amplifier and its of the voltage follower respectively.

And we get from the charge conservation:

$$V_o = \frac{2V_i - DV_R}{\frac{A_2}{A_2+1} + \frac{2}{A_1} + \frac{C_{in}}{CA_1}} = \frac{2V_i - DV_R}{\frac{A_2}{A_2+1} + \frac{2}{A_1^*}} \tag{5.15}$$

where A_1^* is given by 5.12. The ideal behavior is obtained when the denominator is equal to 1: this happens when the gains A_1 and A_2 are in the relationship

$$A_1^* = 2(A_2 + 1) \tag{5.16}$$

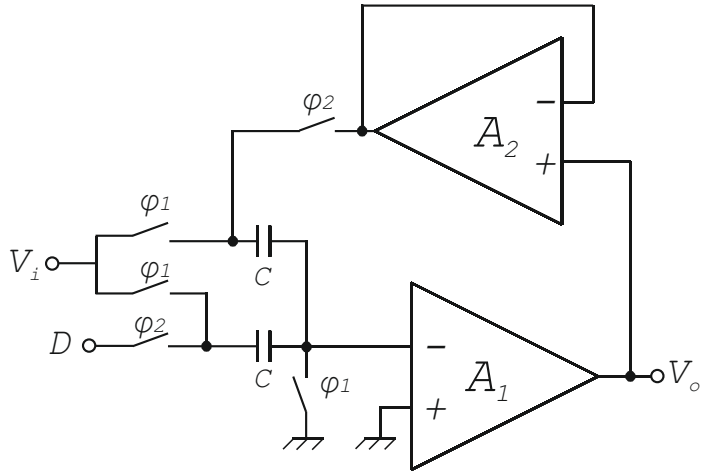

Figure 5.6. Active feedback loop applied to 1.5bit MDAC

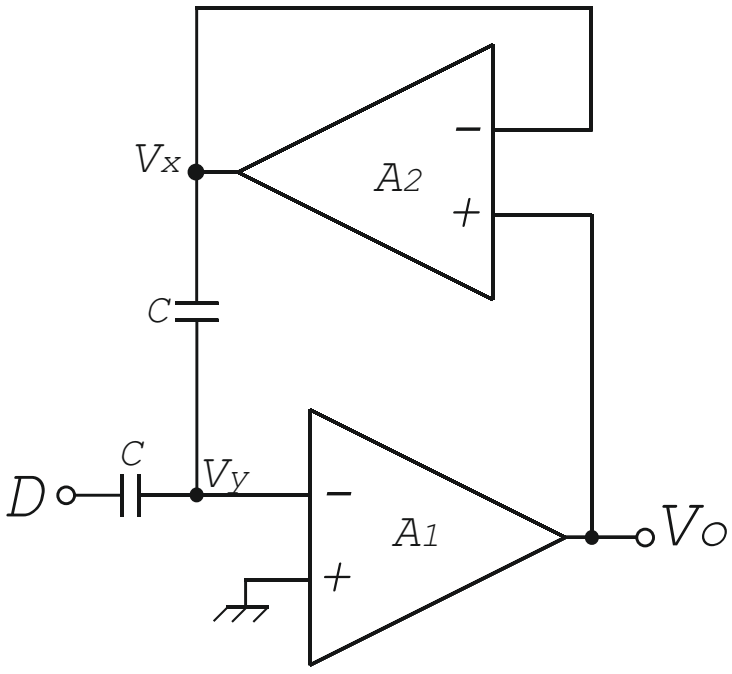

Figure 5.7. Equivalent circuit of an active-feedback MDAC in hold phase

and completely desensitizes the MDAC from the effect of finite gain of the opamp. (5.16) is independent from the absolute values of the gains, thus the ideal behavior for the MDAC can be achieved even in case of very low-gain opamps, if (5.16) is satisfied.

5.1.5 Figure of Merit for Active Feedback Structure

As precedently described, the gain error in the active feedback structure can be mathematically set to zero if a perfect matching condition between the gains of the opamps is reached. In the physical implementation of the circuit, different causes can affect this relationship, consequently, a reduced residual gain error effect remains. In order to compare the performance of this structure, with that obtained by the classical feedback we named A_{eq} the equivalent gain wich must have an operational amplifier in a classical feedback loop to produce a gain error equal to the residual gain error of the active feedback structure. An opamp with A_{eq} gain, closed in a feedback loop with 1/2 feedback ratio cause a gain error of

$$err_{std} = \frac{4}{2 + A_{eq}} \tag{5.17}$$

5.1.6 Mismatch on Gain of Opamps

In the previous section, the ideal condition for the desensitisation of the MDAC from the finite gain effect was stated. In the actual implementation different parasitic effects do not allow the precise matching between the gains of the opamps. Under the non-ideal condition, only a partial desensitisation can be reached. In this section the effects of not perfect relation $A_1^* = 2(A_2 + 1)$ are investigated. More precisely at the system level the effects of error in "x2" and in "+2" in the relation can be separately investigated.

5.1.6.1 "+2 Error"

As first, we consider the case where the main operational amplifier has a gain value A_1 different to the ideal value required to obtain the gain error cancellation. With the assumption that the error is only in +2 of the formula:

$$A_1 = 2(A_2 + 1) + \epsilon_{+2} \tag{5.18}$$

where ϵ_{+2} is the error on "+2" in the gains ratio. Inserting (5.18) in (5.9) we get the effect of the imprecision on the gain error

$$err_{+2} = 2 - \frac{2[2 + 2A_2 - 2(1 + A_2) - \epsilon_{+2}]}{[2(1 + A_2) + \epsilon_{+2}]A_2 + 2(A_2 + 1)} = \frac{-2\epsilon_{+2}}{2(1 + A_2)^2 + A_2\epsilon_{+2}} \tag{5.19}$$

From (5.19) and (5.17) the equivalent gain A_{eq} can be calculated, and we obtain

$$A_{eq+2} = -\frac{2[2(A_2+1)^2 + A_2\epsilon_{+2}]}{\epsilon_{+2}} - 2 \tag{5.20}$$

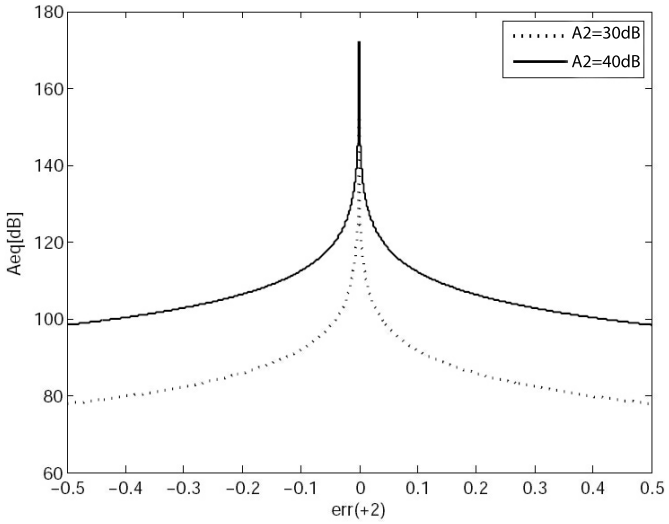

Figure 5.8. Equivalent gain vs error in +2. The value of $A_1 \cdot A_2$ is 66dB when A_2 is 30dB and 86dB when A_2 is 40dB

Figure 5.8 shows the equivalent gain for different values of A_2 and ϵ_{+2}, and we can see that also for low voltage gain of the opamps the equivalent gain is always above the product of the gain of the involved opamps. In particular the value of the equivalent gain approaches asymptotically infinite when the error is nearby zero.

5.1.6.2 "x2 Error"

As the "+2 error" case, now the gain of the main operational amplifier with an error in the x2 term respect the ideal value is considered. In this case is made the hypothesis which all the error is due to the "x2" of the relation $A_1 = 2(A_2 + 1)$, in this case the gain of the main amplifier is:

$$A_1 = 2(1 + \epsilon_{x2})(A_2 + 1) \tag{5.21}$$

where ϵ_{x2} is the error committed on x2. Combining (5.21) with (5.9), we get the effect of non-perfect x2 in the relation on the gain error of the structure

$$err_{x2} = \frac{2[2 + 2A_2 - 2(1+\epsilon_{x2})(1+A_2)]}{[2(1+\epsilon_{x2})(1+A_2)]A_2 + 2(A_2+1)} = \frac{-4\epsilon_{x2}}{2[(1+A_2) + A_2\epsilon_{x2}]} \tag{5.22}$$

The equivalent gain A_{eq} that takes into account the "x2" error can be found by $err_{std} = err_{x2}$:

$$\frac{4}{2+A_{eq}} = \frac{-4\epsilon_{x2}}{2[(1+A_2)+A_2\epsilon_{x2}]} \rightarrow A_{eq} = -\frac{2(A_2+1)(1+\epsilon_{x2})}{\epsilon_{x2}} \tag{5.23}$$

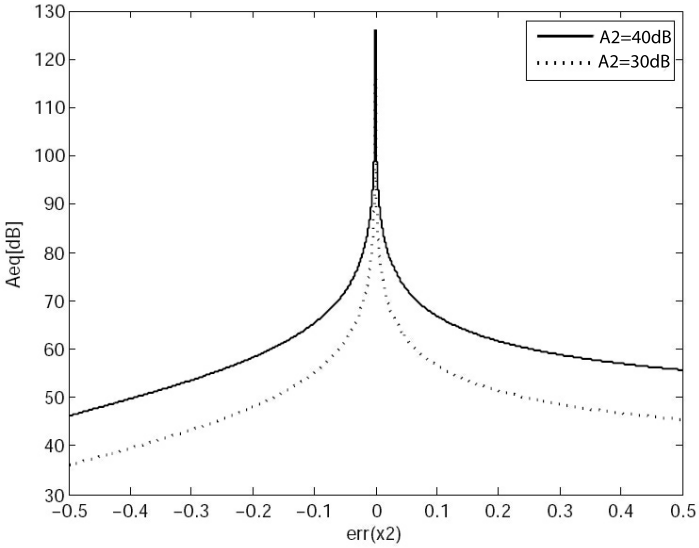

Figure 5.9. Equivalent gain vs "x2" error. The value of $A_1 \cdot A_2$ is 66dB when A_2 is 30dB and 86dB when A_2 is 40dB

Figure 5.9 show the effect of the "x2" error on equivalent gain A_{eq} for different values of A_1. Obviously the "x2" error is more critical than "+2" error.

5.1.6.3 Error Model

In the previous two cases the "x2 " and "+2" errors were taken into account separately. This kind of approach is very usefull to understand which of the considered effects mainly affects the equivalent gain A_{eq}. In a real implementation both the errors are present at the same time in the structure, then a model that takes into account both the error is required for a correct modeling of the circuit. The relation between the gain of the involved opamps can be written as:

$$A_1 = 2(1+\epsilon_{x2})(A_2+1) + \epsilon_{+2} \tag{5.24}$$

substituting the (5.24) in (5.9) we get the MDAC gain error

$$err_{tot} = -\frac{2[2\epsilon_{x2}(A_2+1)+\epsilon_{+2}]}{2(A_2+1)^2 + 2A_2(A_2+1)\epsilon_{x2} + A_2\epsilon_{+2}} \tag{5.25}$$

and the equivalent gain is given by

$$A_{eq} = -\frac{2[2(A_2+1)^2 + 2A_2(A_2+1)\epsilon_{x2} + A_2\epsilon_{+2}]}{2\epsilon_{x2}(A_2+1)+\epsilon_{+2}} - 2 \tag{5.26}$$

5.1.7 Analysis of the Offset in the MDAC

In all the analog circuits an offset error always exists because it is related to the mismatch between the devices that occours during the fabrication phase. The offset effect should be taken into account, in particular in low voltage applications. A model solution to take into account the offset of the opamp is to consider it as ideal, placing in series to the input an offset voltage generator as shown in figure5.10.

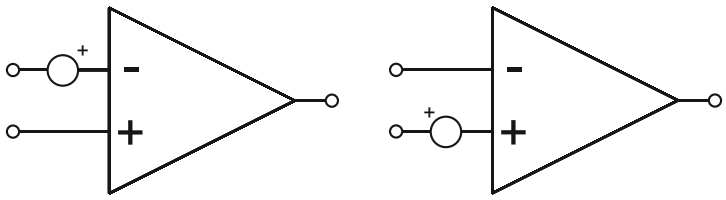

Figure 5.10. Input referred noise generators

The offset is a linear error in the single stage of the pipeline ADC, but generates a non-linear variation on the transcaracteristic of the converter. In the following of this subsection the effect of the offset for the classical MDAC topology, and for the proposed active-feedback based MDAC are studied, and two possilbe ways to overcome this effect in active feedback topology are proposed.

5.1.7.1 Offset in Classical MDAC Topology

Figure 5.11 show the equivalent circuit for the hold phase of the Sample-and-Hold that takes into account the offset effect of the opamp.

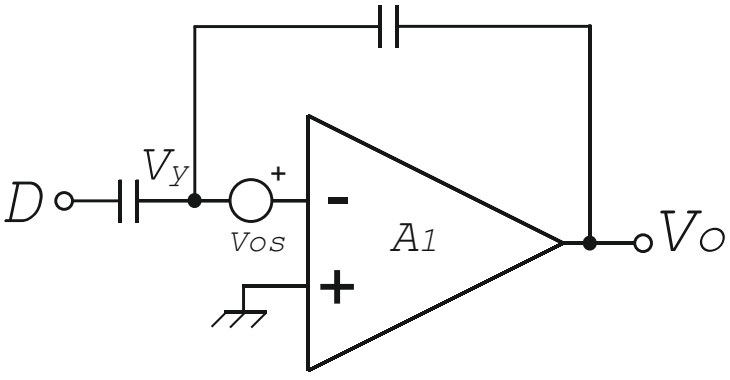

Figure 5.11. Classical feedback MDAC stage in hold phase with offset generator

The charge during the sampling phase is due to:

$$Q_S = 2V_iC \tag{5.27}$$

and then during the hold phase is:

$$Q_H = C\left(D + \frac{V_o}{A} + V_{os}\right) + C\left(V_o + \frac{V_o}{A_1} + V_{os}\right) \tag{5.28}$$

Exploiting the charge conservation between the two phases we obtain:

$$Q_S = Q_H \rightarrow 2V_i = D + 2V_{os} + V_o\left(1 + \frac{2}{A}\right) \tag{5.29}$$

thus the output voltage is

$$V_o = \frac{2V_i - D + 2V_{os}}{\left(1 + \frac{2}{A}\right)} = G(2V_i - D) + K \tag{5.30}$$

Where K represents the offset contribution, and it is equal to:

$$K = 2V_{os}\frac{A}{A+2} \tag{5.31}$$

when the gain of the opamp is high the offset contruibution becomes

$$A \rightarrow \infty \qquad K \approx 2V_{os} \tag{5.32}$$

thus offset cancellation techniques are required to eliminate the offset, because the feedback loop is not able to cancel the opamp offset.

5.1.7.2 Correlated Double Sampling on Classical MDAC Topology

Different solutions to eliminate the offset of the opamp are available in literature, one of these techniques is called Correlated Double Sampling (CDS). In this technique the offset voltage is precharged on the sampling capacitors during the sampling phase, and then will be subtracted during the hold phase. The schematic of the MDAC with CDS is shown in figure 5.12.

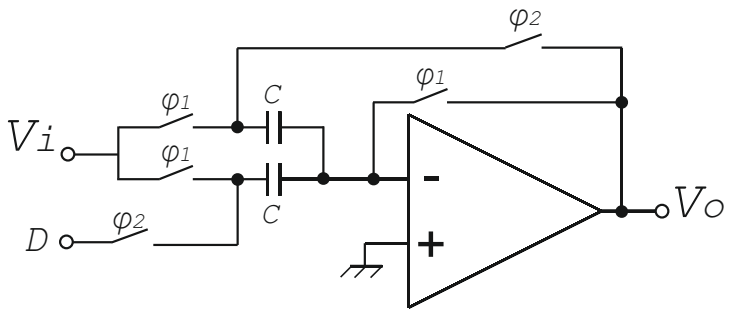

Figure 5.12. 1.5 bit MDAC with CDS

The equivalent circuit during the sampling phase is shown in figure 5.13.

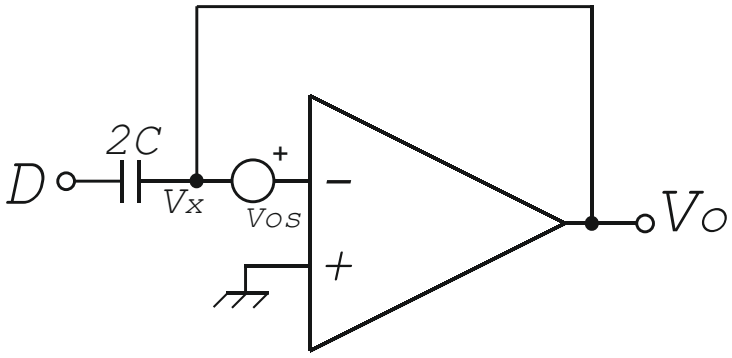

Figure 5.13. Correlated Double Sampling applied on classical feedback MDAC

The charge collected during the sampling phase is

$$Q_S = 2C(V_i - V_x) \tag{5.33}$$

where

$$V_x = -V_{os} - \frac{V_x}{A} \rightarrow V_x\left(1 + \frac{1}{A}\right) = -V_{os} \rightarrow V_x = -V_{os}\frac{A}{1+A} \tag{5.34}$$

and then we can write the total charge collected during the sampling phase as

$$Q_S = 2C\left(V_i + V_{os}\frac{A}{1+A}\right) \tag{5.35}$$

During the hold phase the total charge is given by:

$$Q_H = C\left[D + 2V_{os} + V_o\left(1 + \frac{2}{A}\right)\right] \tag{5.36}$$

and exploiting the charge conservation during the two phases we get:

$$Q_S = Q_H \Rightarrow 2V_i + 2V_{os}\frac{A}{1+A} = D + 2V_{os} + V_o\left(1 + \frac{2}{A}\right) \tag{5.37}$$

thus the output voltage is

$$V_o = \frac{2V_i - D + 2V_{os}\left(\frac{A}{1+A} - 1\right)}{1 + \frac{2}{A}} = G(2V_i - D) + K \tag{5.38}$$

where K is the offset contribution, and is equal to:

$$K = \frac{A}{A+2}\left(\frac{2V_{os}\left(\frac{A}{1+A} - 1\right)}{1 + \frac{2}{A}}\right) \qquad A \rightarrow \infty \qquad \longrightarrow K \approx 0 \tag{5.39}$$

Thus the offset contribution is negligible when CDS technique is applied.

5.1.8 Offset in Active-Feedback MDAC Topology

To study the effect of the offset in the active feedback loop the contributions of the two opamps should be treated separately. In the proposed topology the offset source is present only during the hold phase, as shown in figure 5.14

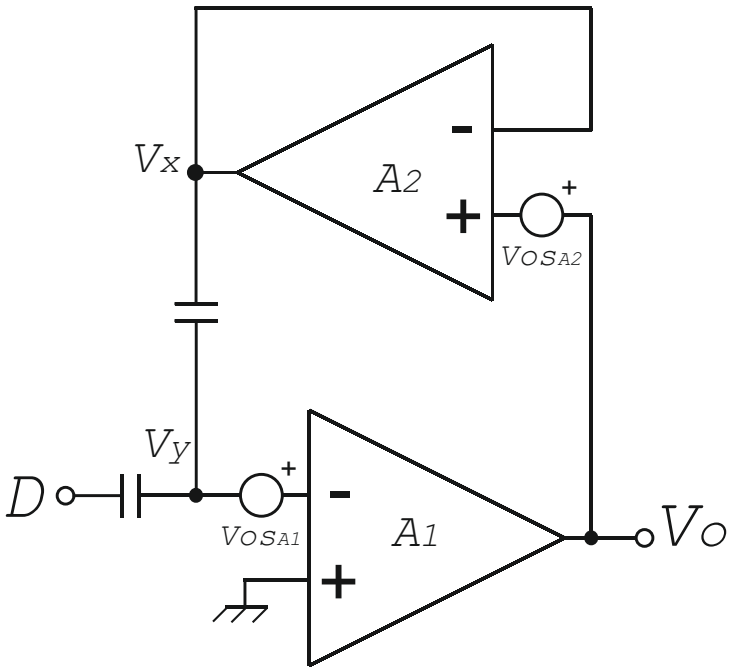

Figure 5.14. Active-feedback based MDAC in hold phase with offset generators

Naming $V_x = (V_o - V_{osA_2})\frac{A_2}{A_2+1}$ and $V_y = -\frac{V_o}{A_1} - V_{osA_1}$, the charge collected during the hold phase is

$$Q_H = C(D-V_y)+C(V_x-V_y) = CD+V_oC\left(\frac{2}{A_1}+\frac{A_2}{1+A_2}\right)+2CV_{osA_1}-C\frac{A_2}{1+A_2}V_{osA_2} \tag{5.40}$$

and exploiting the charge conservation during the two phases we can get the output voltage as:

$$V_o = \frac{2V_i - D - 2V_{osA_1} + \frac{A_2}{1+A_2}V_{osA_2}}{\frac{2(1+A_2)+A_1A_2}{A(1+A_2)}} = G(2V_i - D) + K \tag{5.41}$$

where K is the offset contribution

$$K = \frac{A_1(1+A_2)}{2(1+A_2)+A_1A_2}\left(-2V_{osA_1} + \frac{A_2}{1+A_2}V_{osA_2}\right) \tag{5.42}$$

considering high values for the gain of both the opamps

$$A_1, A_2 \to \infty \qquad K \approx -2V_{osA_1} + V_{osA_2} \tag{5.43}$$

Thus on the output of the active feedback loop we find the offset voltage of both the opamps, for this reason a technique to cancel the offset of the opamps is required. The CDS can be applied on the active feedback loop in two different ways: only on the main amplifier, or on the whole chain.

5.1.8.1 CDS Applied on the Main Amplifier of the Active Loop

As said for the classical configuration, in the CDS technique the offset is sampled during the sampling phase, and then is subtracted during the hold phase (or error amplification when is applied in an MDAC). A possible way is to apply the CDS technique only on the main amplifier of the active feedback loop. In figure 5.15 is shown the schematic of this solution.

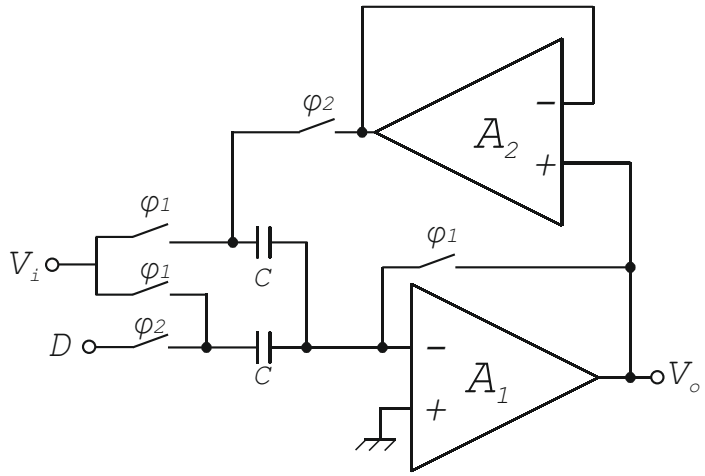

Figure 5.15. CDS applied on the main amplifier of the active feedback loop

The equivalent circuit for the sampling phase is shown in figure 5.16
The total charge collected during this phase is $Q_S = 2C(V_i - V_y)$ where

$$V_y = -V_{osA_1} - \frac{V_y}{A_1} \rightarrow V_y\left(1 + \frac{1}{A_1}\right) = -V_{osA_1} \rightarrow V_y = -V_{osA_1}\frac{A_1}{1 + A_1} \tag{5.44}$$

During the error amplification phase the total charge is given by (5.36), thus by applying the charge conservation between the two phases we get

$$Q_S = Q_H \Rightarrow 2\left(V_i + \frac{V_{osA_1}}{1 + \frac{1}{A_1}}\right) = D + V_o\left(\frac{2}{A_1} + \frac{A_2}{1 + A_2}\right) + 2V_{osA_1} - \frac{A_2}{1 + A_2}V_{osA_2} \tag{5.45}$$

From the latter equation, the output voltage can be obtained

$$V_o = \frac{2V_i - D + 2V_{osA_1}\left(\frac{A_1}{A_1+1} - 1\right) + \frac{A_2}{1+A_2}V_{osA_2}}{\frac{2(A_2+1)+A_1A_2}{A_1(1+A_2)}} = G(2V_i - D) + K \tag{5.46}$$

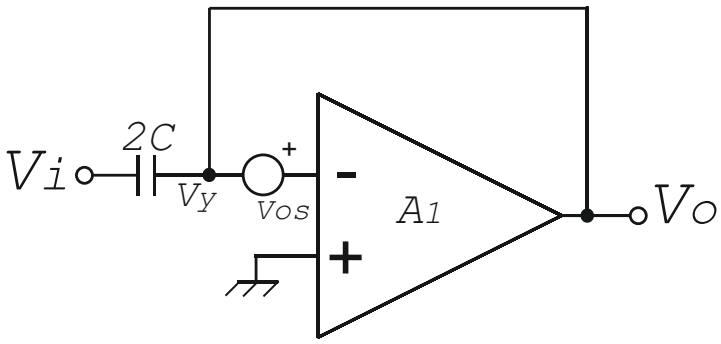

Figure 5.16. Correlated Double Sampling applied on the main amplifier of an active-feedback based MDAC during the sampling phase

where K is the offset contribution, and is equal to

$$K = \frac{A_1(A_2+1)}{2(A_2+1)+A_1A_2}\left[2V_{osA_1}\left(\frac{A_1}{A_1+1}-1\right)+\frac{A_2}{A_2+1}V_{osA_2}\right] \tag{5.47}$$

considering high gain for both the opamps the residue offset effect is

$$A_1, A_2 \to \infty \qquad \longrightarrow \qquad K = V_{osA_2} \tag{5.48}$$

Thus, if the CDS is applied only on the main opamp, the offset contribution of the opamp involved in the feedback path is not canceled.

5.1.8.2 CDS Applied on Active Loop

The CDS technique can be applied also at the whole active loop as shown in figure 5.17

The equivalent schematic of the hold phase is shown in figure 5.18.

Where the voltage $V_x = \frac{A_2}{1+A_2}(V_o - V_{osA_2})$ and $V_o = -A_1(V_x - V_{osA_1})$ thus we can write

$$V_x = \left[\frac{1+A_2}{1+A_2+A_1A_2}\left(-\frac{A_2}{1+A_2}\left(A_1V_{osA_1}+V_{osA_2}\right)\right)\right] \tag{5.49}$$

The total charge collected during the sample phase is

$$Q_S = 2C(V_i - V_x) = 2C\left(V_i + \frac{A_1A_2V_{osA_1}+A_2V_{osA_2}}{1+A_2+A_1A_2}\right) \tag{5.50}$$

and applying the conservation of the charge during the two phases we get

$$Q_S = Q_H \Rightarrow 2C\left(V_i + \frac{A_1A_2V_{osA_1}+A_2V_{osA_2}}{1+A_2+A_1A_2}\right) = D+V_o\left(\frac{2}{A_1}+\frac{A_2}{1+A_2}\right)+2V_{osA_1}-\frac{A_2}{1+A_2}V_{osA_2} \tag{5.51}$$

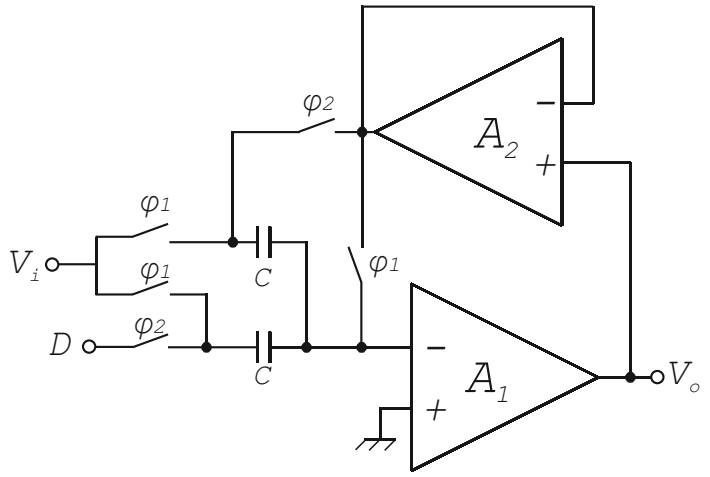

Figure 5.17. CDS aplied on the whole active feedback loop

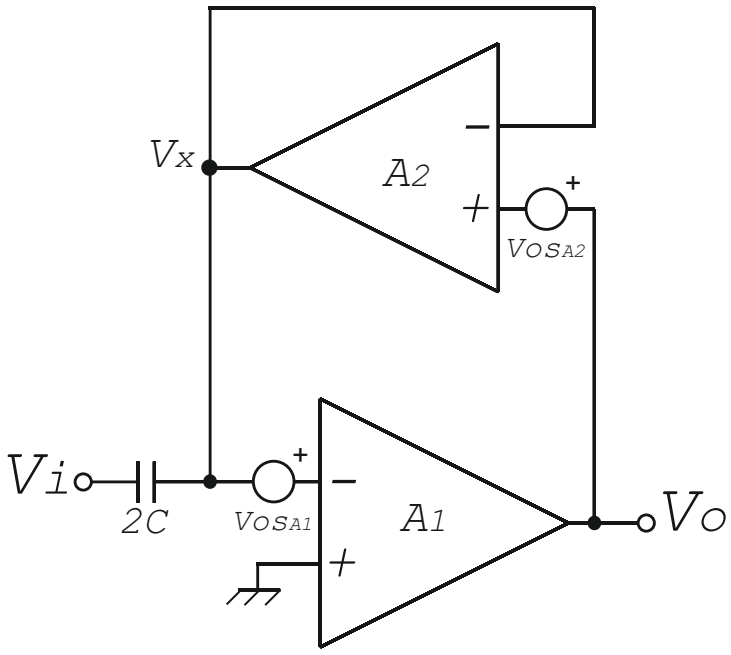

Figure 5.18. Correlated Double Sampling applied on the whole active feedback loop.

From the latter equation the output voltage can be found:

$$V_o = \frac{2V_i - D + 2\left(\frac{A_1A_2V_{osA_1}+A_2V_{osA_2}}{1+A_2+A_1A_2}\right) - 2V_{osA_1} + \frac{A_2}{1+A_2}V_{osA_2}}{\frac{2}{A_1}+\frac{A_2}{1+A_2}} = G(2V_i - D) + K \tag{5.52}$$

where K is the contribution of the offset, and its value is

$$K = \left[2V_{osA_1}\left(\frac{A_1A_2}{1+A_2+A_1A_2} - 1\right) + V_{osA_2}\left(\frac{2A_2}{1+A_2+A_1A_2} + \frac{A_2}{1+A_2}\right)\right]\frac{A_1(A_2+1)}{1(A_2+1)+A_1A_2} \tag{5.53}$$

for high gain values of the amplifiers we get

$$A_1, A_2 \to \infty \qquad \longrightarrow \qquad K \approx V_{osA_2} \tag{5.54}$$

This result hightlights that also including the feedback opamp in the CDS does not bring any advantage and its offset voltage is not canceled.

5.1.9 Offset Cancellation by Auxiliary Capacitor in Active-Feedback Topology

As proved in the latter subsections the CDS is not sufficient to cancel the offset of both the opamps, in particular the offset of the opamp involved in the feedback branch can not be deleted by the CDS. To overcome this limitations it is possible to apply the CDS on the main amplifier and use an auxiliary capacitor to precharge the offset of the feedback amplifier during the sampling phase. It can be done because during the sampling phase the feedback amplifier is not involved. The proposed schematic is shown in figure 5.19

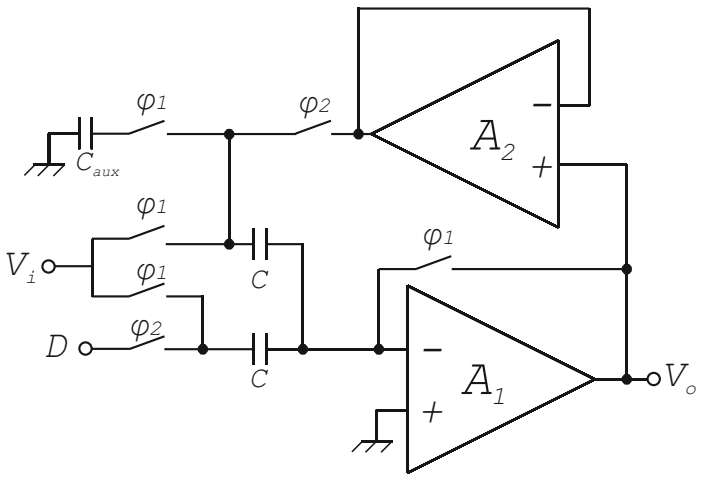

Figure 5.19. Offset cancellation by auxiliary capacitor

Then during the hold phase the offset voltage stored in the auxiliaty capacitor is subtracted from the output.

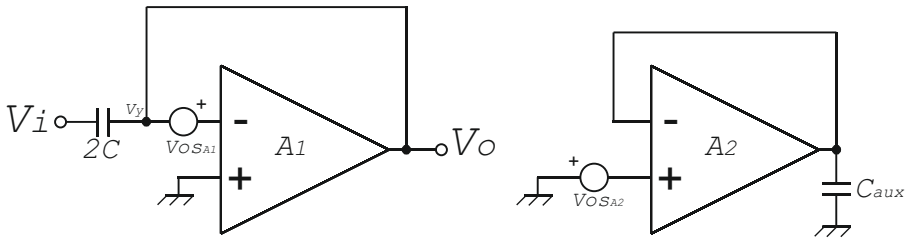

Figure 5.20. Offset cancellation by auxiliary capacitor applied to active-feedback loop during the sampling phase

In figure 5.20 the equivalent circuit during the sampling phase is shown. The voltage on the auxiliary capacitance C_x is:

$$V_{C_x} = -V_{osA_2}\frac{A_2}{1+A_2} \tag{5.55}$$

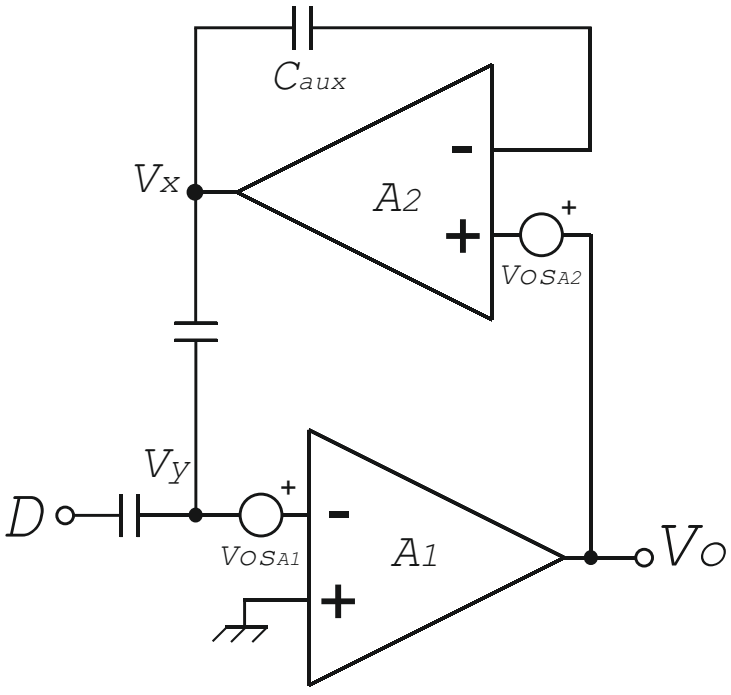

Figure 5.21. Offset cancellation by auxiliary capacitor applied to active-feedback loop during the hold phase

The circuit during the hold phase is shown in figure 5.21, where

$$V_x = V_o \frac{A_2}{A_2+1} - V_{osA_2} \frac{A_2}{(A_2+1)^2} \tag{5.56}$$

The charge during the sampling phase is

$$Q_S = 2C\left(V_i - \frac{V_{osA_1}}{1+\frac{1}{A_1}}\right) \tag{5.57}$$

indeed, during the hold phase the charge collected is

$$Q_H = C(D - V_y) + C(V_x - V_y) = CD - 2CV_y + CV_x \tag{5.58}$$

From (5.56) and (5.58) we get:

$$Q_H = C\left[D + 2\left(\frac{V_o}{A_1} + V_{osA_1}\right) + V_o\frac{A_2}{A_2+1} - \frac{A_2}{(A_2+1)^2}V_{osA_2}\right] \tag{5.59}$$

and applying the charge conservation during the two phases we obtain the output voltage as

$$V_o = \frac{2V_i - D + V_{osA_1}\left(\frac{A_1}{A_1+1} - 1\right) + V_{osA_2}\frac{A_2}{(A_2+1)^2}}{\frac{2}{A_1} + \frac{A_2}{A_2+1}} = G(2V_i - D) + K \tag{5.60}$$

where K represents the offset contribution:

$$K = \left[-V_{osA_1}\left(\frac{1}{1+A_1}\right) + V_{osA_2}\frac{A_2}{(A_2+1)^2}\right]\frac{A_1(A_2+1)}{A_1A_2 + 2(A_2+1)} \tag{5.61}$$

then for high values of gain the offset contrinution is equal to zero. This demostrates that the CDS with an auxiliary capacitor it is able to cancel the offset of both the opamps.

5.1.10 Offset Pre-Sampling in Active-Feedback Topology

Starting from the previous solution that uses an auxiliary capacitor to precharge the offset value, the active feedback has been modified in order to precharge the offsets on the sampling capacitors, and thus avoid auxiliary capacitors. Figure 5.22 shows the schematic of the proposed solution.

In figure 5.23 the equivalent circuit during the sampling phase is shown, where $V_y = -\frac{V_{osA_1}}{1+\frac{1}{A_1}}$, and the charge collected during the sampling phase is:

$$Q_S = C\left[V_i\left(\frac{A_2}{1+A_2}+1\right) + 2V_{osA_1}\frac{A_1}{A_1+1} - V_{osA_2}\frac{A_2}{A_2+1}\right] \tag{5.62}$$

For the charge conservation during the two phases we get the output voltage

$$V_o = V_i\frac{2A_2+1}{1+A_2} - D + V_{osA_1}\left(\frac{2A_1}{A_1+1} - 2\right) - V_{osA_2}\left(\frac{A_2}{A_2+1} - \frac{A_2}{A_2+1}\right) \cong G(2V_i - D) + K \tag{5.63}$$

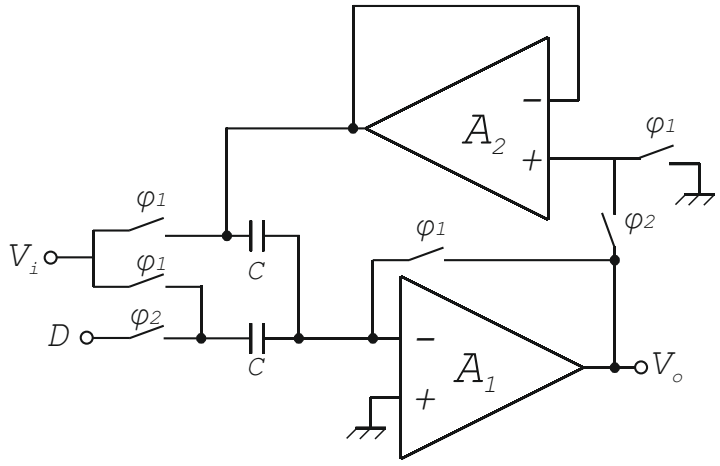

Figure 5.22. Offset pre-sampling in active feedback loop

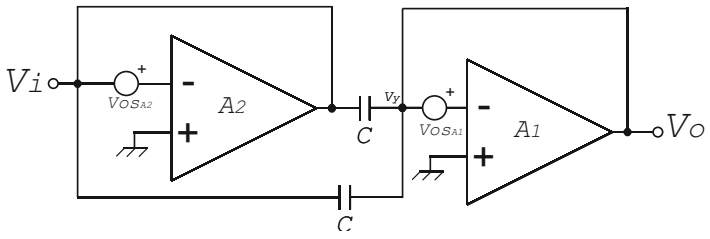

Figure 5.23. Offset presampling

where the offset contribution K is

$$K = V_{osA_1}\left(\frac{2A_1}{A_1+1}-2\right) \quad \text{for} \quad A_1 \to \infty \quad \longrightarrow \quad K \approx 0 \tag{5.64}$$

This solution is able to delete the offset contribution of both the opamps without involving auxiliary capacitors. In all the proposed solutions to delete the offset contribution we need high gain of the opamps, thus even if the acrive feedback loop is theoretically able to delete the gain error of the opamp also for very low gain values, the offsets could pose minimum acceptable values for the gains of the opamps.

5.2 Frequency Analysis of the Active-Feedback Loop

Guaranteeing the stability of each amplifier involved in the active-feedback loop should be not sufficient to obtain the stability of the whole system, thus a frequency analysis of the active feedback loop is required to get the frequency constraints of the involved opamps needed to obtain the stability of the system. In fact, during the hold phase the opamps are connected in a closed loop, that might be unstable if the poles of the opamps are too close respect to the unity gain frequency. Thus the open loop poles of each opamp must be fixed on a well precise place of the root locus. Furthermore, general design rules that links the opamps constraints to the system requirement is useful to a proper design of the system. In this subsection a single pole approximation, and a more accurate two poles approximation model are used to extract the relationship between phase margin and bandwidth of the opamps and those required by the system, useful during the design of the active feedback structure. In order to simplify the notation, from now on out, the main amplifer with gain A_1 is named "A", and the feedback amplifier with gain A_2 is named "B".

5.2.1 Single Pole Approximation

As first a single pole transfer function approximation can be used to describe the frequency behaviour of the opamps

$$A(s) = \frac{A_0}{1+s\tau_A} = \frac{A_0}{1+\frac{s}{p_A}} \tag{5.65}$$

$$B(s) = \frac{B_0}{1+s\tau_B} = \frac{B_0}{1+\frac{s}{p_B}} \tag{5.66}$$

the opamp "B" is closed as negative unitary gain voltage buffer, thus:

$$B_F(s) = \frac{B_{F0}}{1+s\tau_{B_F}} = \frac{B_{F0}}{1+\frac{s}{p_{B_F}}} \tag{5.67}$$

where $B_{F0} = \frac{B_F}{1+B_F}$ and $\omega_{\tau_F} = \omega_T(1+B_F)$. From the latter equations the unity gain frequency of the overall loop can be determined

$$|T(\omega_0)| = \beta\,|A(\omega_0)\,||\,B_F(\omega_0)| = \frac{1}{2}\frac{A_0}{\sqrt{1+\omega_0^2\tau_A^2}}\frac{B_{F0}}{\sqrt{1+\omega_0^2\tau_{BF}^2}} = 1 \tag{5.68}$$

Where β is the feedback factor and in this case its value is 1/2. In the case that the pole of the opamp B is negligible, because the unitary feedback moves the pole to higher frequency by a factor $1+B$, the loop gain can be written as:

$$|T(\omega_0)| = \frac{A_0 B_{F0}}{2}\frac{1}{\sqrt{1+\omega_0^2\tau_A^2}} = 1 \tag{5.69}$$

from which the ω_0 can be determined

$$\omega_0 = \frac{1}{\tau_A}\sqrt{\left(\frac{A_0 B_{F0}}{2}\right)^2 - 1} \cong \frac{A_0 B_{F0}}{2\tau_A} = \frac{2(B+1)\frac{B}{B+1}}{2\tau_A} = \frac{B}{\tau_A} \tag{5.70}$$

If the dominant pole hypothesis is valid, the phase contribution of the first pole (due to opamp A) is 90° at ω_0. Thus the phase margin of the whole system m_{φ_S} poses a constraint on the ratio between the bandwidt of the two opamps:

$$m\varphi_S = 180 - \angle T(\omega_0) \cong 90 - \arctan(\omega_0\tau_{B_F}) \tag{5.71}$$

thus from 5.71 follows

$$\tan(90 - m\varphi_S) = \omega_0\tau_{B_F} \tag{5.72}$$

The latter one links the frequency of the opamp B's pole with the phase margin of the system

$$\begin{aligned} \tau_{BF} &= \frac{\tau_B}{1+B} = \frac{1}{\omega_0}\tan(90 - m\varphi_S) = \frac{\tau_A}{B}\tan(90 - m\varphi_S) \\ \tau_B &= \frac{1+B}{B}\tau_A\tan(90 - m\varphi_S) \end{aligned} \tag{5.73}$$

where $\omega_0 = \frac{B}{\tau_A}$, derived from (5.70) was considered. From (5.73) and (5.70), the ω_{uB} can be found as:

$$\begin{aligned} \omega_{uB} = \frac{B}{\tau_B} &= \frac{B}{\frac{1+B}{B}\tau_A\tan(90 - m\varphi_S)} = \frac{B^2}{1+B}\frac{1}{\tau_A}\frac{1}{\tan(90 - m\varphi_S)} = \\ &= \omega_{uA}\frac{B^2}{2(B+1)^2}\frac{1}{\tan(90 - m\varphi_S)} \end{aligned} \tag{5.74}$$

Finally it leads to an expression suitable for the design of the opamps.

$$\frac{\omega_{uB}}{\omega_{uA}} = \frac{1}{2}\left(\frac{B}{1+B}\right)^2\frac{1}{\tan(90 - m\varphi_S)} \tag{5.75}$$

the latter one brings with it the relationship between the poles of the system:

$$\frac{p_B}{p_A} = \frac{\omega_{uB}}{\omega_{uA}}\frac{A_0}{B} = \frac{\omega_{uB}}{\omega_{uA}}\frac{2(B+1)}{B} \approx 2\frac{\omega_{uB}}{\omega_{uA}} \tag{5.76}$$

5.2.2 Two Poles Approximation

The signle pole approximation can be adopted only when the second pole of the opamp is well spaced from the first one, this mean more than one order of magniude. However, it may not always be possible, thus more accurate two poles model is required to describe the opamps. The open-loop transfer function of the opamp "B" is:

$$B(s) = \frac{B_0}{(1+s\tau_{1B})(1+s\tau_{2B})} \tag{5.77}$$

If the dominant pole condition is verified, the first pole τ_{1B} is related to the unitary gain bandwidth ω_{uB} and the gain B:

$$\frac{1}{\tau_{1B}} = \frac{\omega_{uB}}{B_0} \tag{5.78}$$

The phase margin brings information on the distance between the poles of the opamp:

$$m\varphi_B = 180 - \varphi_{TOT_B}(\omega_{u_B}) = 180 - (\varphi_{1B} + \varphi_{2B}) \tag{5.79}$$

where $m\varphi_B$ is the phase margin of the feedback amplifier, φ_{TOT_B} the total phase contribution of its poles calculated at the unity gain frequency, and φ_{1B} and φ_{2B} are the phase contribution at the unity gain frequency given by the first and second pole. When dominant pole condition is verified, the phase contribution of the first pole at ω_{uB} can be considered 90° , thus (5.79) becomes:

$$m\varphi_B = 90 - arctan\,(\omega_{uB}\tau_{2B}) \tag{5.80}$$

thus:

$$\tau_{2B} = \frac{1}{\omega_{uB}} tan\,(90 - \varphi_B) \tag{5.81}$$

The opamp B is used in unitary gain feedback during the hold phase, thus the closed loop trasnfer function must be considered:

$$B_F = \frac{B_0}{(1+s\tau_{1B})(1+s\tau_{2B}) + B_0} \rightarrow \frac{B_0}{\underbrace{1-\omega^2\tau_{1B}\tau_{2B} + B_0}_{\Re} + J\underbrace{\omega(\tau_{1B}+\tau_{2B})}_{\Im}} \tag{5.82}$$

and then:

$$\angle B_F = -arctan\left[\frac{\omega(\tau_{1B}+\tau_{2B})}{1-\omega^2\tau_{1B}\tau_{2B}+B_0}\right] \tag{5.83}$$

In the same way, some observations on the opamp A are useful. First of all, also the tranfer function of the opamp A is described with two poles.

$$A(s) = \frac{A_0}{(1+s\tau_{1A})(1+s\tau_{2A})} \tag{5.84}$$

Furtermore it can be supposed that the first pole of the opamp A is also the first pole of the whole active feedback system, since $A_0 > B_0$ and the opamp B is closed in unity-gain feedback. Under the dominant pole assumption, the ω_0 of the whole system is due to the product of the first pole for the open loop gain of the whole system

$$\omega_0 = p_{1A}\cdot A\frac{B_0}{1+B_0} = p_{1A}\cdot 2(B_0+1)\frac{B_0}{1+B_0} = 2B_0p_{1A} \tag{5.85}$$

From the latter one the ω_{uA} of the main amplifier can be obtained

$$\omega_{uA} = Ap_{1A} = \underbrace{2(B_0+1)}_{A}\underbrace{\frac{\omega_0}{2B_0}}_{p_{1A}} = \omega_0\left(\frac{B_0+1}{B_0}\right) = \omega_0\left(1+\frac{1}{B_0}\right) \tag{5.86}$$

The second pole is given by:

$$p_{2A} = \frac{\omega_{uA}}{tan\,(90-m\varphi_A)} \tag{5.87}$$

and from (5.86) and (5.87) the second pole of the opamp A can be obtained as function of the gain, phase margin and ω_0 as:

$$p_{2A} = \frac{\omega_0\left(1+\frac{1}{B_0}\right)}{tan\,(90-m\varphi_A)} \tag{5.88}$$

The phase margin of the whole active fedback system is a function of the 4 poles considered in the system.

$$m\varphi_S = 180-\varphi_{TOT}(\omega_0) = 180-(\varphi_{1A}+\varphi_{2A}+\angle B_F) \tag{5.89}$$

Considering 90° the phase contrinution of the first pole, (5.89) becomes:

$$90-m\varphi_S = arctan\left(\frac{\omega_0}{p_{2A}}\right)+\angle B_F \tag{5.90}$$

From (5.88) an expression for $\angle B_F$ can be obtained as:

$$\angle B_F = 90-m\varphi_S-arctan\left[\frac{tan\,(90-m\varphi_A)}{1+\frac{1}{B_0}}\right] \tag{5.91}$$

and from (5.83) and (5.91), and taking into account $\tau_1 B = \frac{B_0}{\omega_{uB}}$ and $\tau_2 B = \frac{tan(90-m\varphi_B)}{\omega_{uB}}$ we get:

$$90 - m\varphi_S - arctan\left[\frac{tan\,(90 - m\varphi_A)}{1 + \frac{1}{B_0}}\right] = arctan\left[\frac{\omega(\frac{B_0}{\omega_{uB}} + \frac{tan(90-m\varphi_B)}{\omega_{uB}})}{1 + B_0 - \omega^2 \frac{B_0 tan(90-m\varphi_B)}{{\omega_{uB}}^2}}\right] \tag{5.92}$$

The latter equation may be used for the correct design of the opamps of the system, wheareas the relation between the open loop gains is due to the gain error cancellation.

5.3 Active Feedback Loop in Deep Submicron Technologies

In deep submicron technologies where the intrinsic gain of the devices is quite low, and the system constraints prevent the use of stacked architectures, achieving high gain can be too hard. The active feedback loop does not require high gain opamp structures, but the keyrole is played by the matching between the gains of the involved opamps. In this section an opamp structure that allows to obtain by construction the relationship $A = 2(B + 1)$ between the gains of the opamps is suggested.

5.3.1 Criteria for the topological choice of the opamps

The most common structures to implement opamps are represented by two stages opamp and folded cascode opamp, they provide a gain of $(gm \cdot r_0)^2$. In this case a precise ratio between the open loop gains of the opamps of $A = 2(B + 1)$ is required, thus the choice of the topological architecture is driven by the x2 in the relation between the gain. Obtaining a precise relation between the open loop gains in such structures is too difficult, and the result is very sensitive to the process variations, thus a different structure is required to satisfy the constraint on the gains.

In a current mirror based opamp the voltage gain is due to the product of the transconductance of the input differential pair for the value of the output resistance multiplied for the mirroring factor K_{Mirror} of the current mirror. A schematic block of a Current Mirror Based (CMB) amplifier is shown in figure 5.24.

The voltage gain in CMB opamp is due to:

$$Gain = gmK_{Mirror}R_{Load} \tag{5.93}$$

The Gain Bandwidth Product is due to:

$$\omega_u = \frac{gmK_{Mirror}}{C_{Load}} \tag{5.94}$$

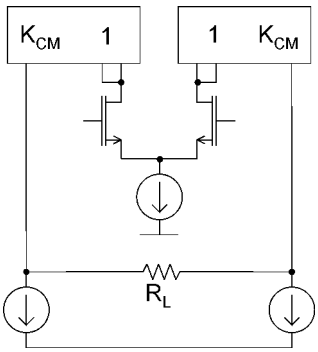

Figure 5.24. Block diagram of a Current Mirror based opamp

Thus it is easy to set a precise gain and bandwidth in CMB structure, for this reason this structure is used as base to develop the opamps for the active feedback loop.

5.3.1.1 Current Mirror Based OPA

A more detailed description of the chosen architecture is reported in this subsection. The figure 5.25 shows the schematic of the CMB opamp.

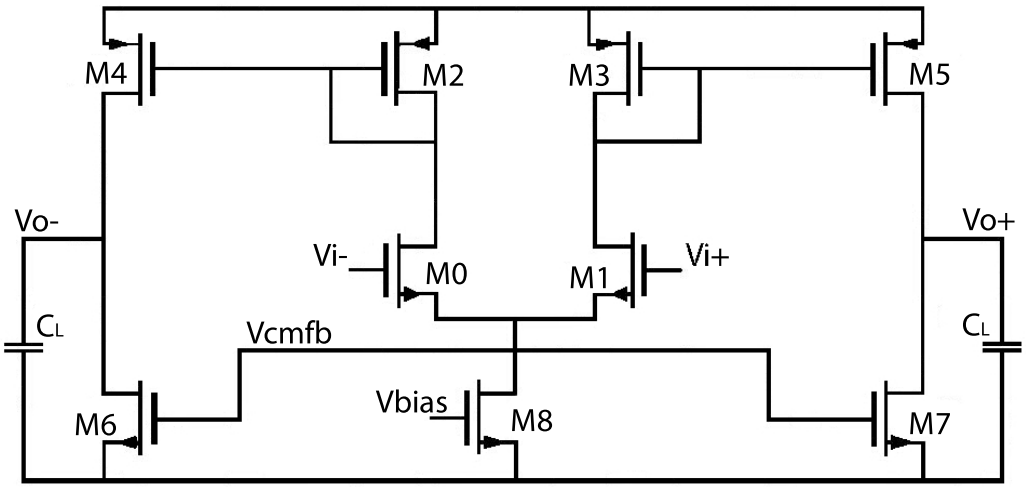

Figure 5.25. Schema base di OPA Current Mirror Based

Eq. (5.94) in this specific case becomes:

$$\omega_u = \frac{K \cdot gm_0}{C_L} \tag{5.95}$$

where gm_0 is the transconductance of the input differential pair M0(M1), K represents the current gain of the current mirror, and C_L is the load capacitance. The non dominant pole is due to the current mirror and can be written as:

$$\omega_2 \approx \frac{gm_2}{C_{gs2} + C_{gs4} + C_{gd4} + C_{gd0} + C_{b2}} \tag{5.96}$$

where gm_2 is the transconductance of the input transistor of the mirrors M2 (M3), C_{gs2} is the parasitic capacitance between gate and source of M2 (M3). C_{gs4} represents the parasitic capacitance between gate and source of MOS M4 (M5), C_{gd0} is the parasitic capacitance between gate and drain of M0 (M1), and C_{b2} is the total substrate capacitance of M2 (M3). The slew rate is given by:

$$SR = \frac{2 \cdot I_{bias6}}{C_L} = \frac{K \cdot I_{bias8}}{C_L} \tag{5.97}$$

where I_{bias6} is the quiescent current of M6 (M7), and I_{bias8} the current of M8. The transconductance of a MOS in saturation region is given by:

$$g_m = \sqrt{2 \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot I_D} = \frac{2 \cdot I_D}{V_{eff}} \tag{5.98}$$

where μ is the carriers mobility, C_{ox} the capacitance for unity area, W/L the form factor of the transistor, I_D the drain current , and V_{eff} the effective gate voltage.

For high resolution applications the thermal noise can be a limiting factor. The noise density of a MOS in saturation region is due to:

$$S(f)|_{MOS} = \frac{8}{3} kT \frac{1}{g_m} \tag{5.99}$$

The input referred spectral noise density of the CMB opamp is given by

$$S(f) = \frac{16}{3} kT \frac{1}{g_{m0}} \left\{ 1 + \frac{g_{m2}}{g_{m0}} + \frac{g_{m4} + g_{m6}}{g_{m0}} \cdot \frac{1}{K^2} \right\} \tag{5.100}$$

where g_{m0},g_{m2},g_{m4} and g_{m6} are the transconductances of M0, M2, M4 and M6 (the factor 2 in the formula is used to take into account M1, M3, M5 and M7), k is the Boltzmann's constant and K the current gain of the mirrors.

5.3.2 Possible Ways to Obtain the Gain Relationship

Satisfying the desired relationship $A = 2(B + 1) = 2B + 2$ between the open loop gains of the involved ompamps itis easiest if the problem is split in two: the first one is how to obtain a x2 in the formula; and the second one, how to obtain the +2.

To obtain the x2 substantially it is possible to act in these ways:

- Exploit the current gain of the current mirror $\mathbf{K}_{Mirror}$.
- Exploit the output resistance $\mathbf{R}_{Load}$.
- Design the first stage with different transconductance **Gm**.

- Exploit additional signal path to obtain the factor 2 independently of **Gm**, **K** and $\mathbf{R}_{Load}$.

5.3.2.1 x2 Based on Current Mirror Ratio

As precedently said the gain of a CMB opamp is given by:

$$Gain = gmK_{Mirror}R_{Load}$$

It is clear that doubling the mirroring factor K leads to a doubling also of the gain. This can be obtained without changing the Gm of the input diffarential pair, or the output resistance R. The main limitation of this solution is due to the difficulties in deep submicrometer technologies to obtain an exact current copy when high values of K are chosen. This means that the mirroring factor does not increase linearly with the transistor's size, it is due to short channel effects, and current partition due to the limited value of output resistance of the MOS in short channel technologies. The value of the output current is described by:

$$I_{OUT} = \frac{(W/L)_2}{(W/L)_1} I_{IN} \left(1 + \frac{V_{DS2} - V_{DS1}}{V_A}\right) \tag{5.101}$$

where V_A is the Early voltage. The systematic error is due to:

$$\epsilon = \frac{V_{DS2} - V_{DS1}}{V_A} \tag{5.102}$$

The Early voltage is a technological parameter, and can not be corrected during the design, it is caused by the channel modulation effect. The Early voltage is given by:

$$V_A = L_{eff} \left(\frac{dX_d}{dV_{DS}}\right)^{-1} \tag{5.103}$$

where L_{eff} is the effective lenght of the channel, and X_d is the lenght of the depleted region of the channel. Thus to overcome errors in a current mirror, both input and output MOS should have the same V_{DS} voltage. The error in the replica growing with the mirroring factor K, this poses a limitation on the maximum mirroring factor, and thus on the gain of the CMB opamp.

5.3.2.2 x2 Based on Load Resistance Ratio

The second parameter that can be modified to obtain the desired ratio between the gains of the ompamps is the load resistence. In this case the opamps are identical, thus the error in the current mirror is avoided because they are biased with the same current, and also the transconductances of the input differential pairs are the same. The load resistance can be implemented in different ways, i.e. thorough an OTA or a Second Generation Current Conveyor (CCII). But when an active circuit is adopted to sintesize an active load, also those poles and zeros must be taken into

account in the transfer funcion of the system, and further, high linearity is required by the involved circuit in order not to worse the linearity of the system. However, regardless to the choice made to implement the resistance, there is an upper limit above which the value of the resistance becomes comparable to the output resistance of the opamp, thus undesired partition effect will appears. This upper limit binds the maximum achiveable gain of the main amplifier, because the other one must see half resistance.

5.3.2.3 x2 Based on Transconductance Ratio

The third variable that can be taken into account to set the gain of a CMB opamp is the transconductance of the input differential pair. Its value is given by:

$$g_m = \mu C_{ox} \frac{W}{L}(V_{GS} - V_{TH})(1 + \lambda V_{DS}) \approx \sqrt{2k' \frac{W}{L} I_D} \tag{5.104}$$

The transconductance is proportional to the square root of the bias current and the form factor of the MOS. Thus to double the g_m the current or the form factor must be quadrupled. Increasing the current leaving unchanged the form factor leads to a variation on the V_{DS} of the MOS, consequently also the voltage of the input branch of the current mirror will be modified, and thus an error on the current copy will appear due to the channel modulation. The same issue will appear if the form factor is modified and the current is constant.

5.3.2.4 x2 Based on Topology

In all the aforementioned solutions there are some issues that make them unsuitable unless changing something in the structure of the CMB topology. A possible way to obtain by construction the desired ratio between the gains of the opamps is by doubling the signal path of the main opamp, and summing in a proper way the signal of the two paths. This allows to obtain exactly the x2 in the formula with the same g_m,K_{Mirror} and R_{Load} for both the opamps. This approach is very useful to extend the active-feedback loop to Sample-and-Hold with xN gain, indeed in this case a generic factor xN between the gains of the opamps is required .

In figure 5.26 is shown the modified structure for the CMB opamp, and the resistive load is left out for practical reasons. In this structure, as in the basic one the input voltage signal is converted in a current signal by the input differential pair M0-M1. The transistors M4 M4' and M5 M5' copy with a factor K the currents that flows respectively in M2 and M3. The current of M4' and M5' in their turn will be copied by two unitary gain current mirror M6'-M6 and M7'-M7 the output branches of this current mirror are connected to the output of the first current mirror: M4 and M5. The current that flows in the additional path(M5'-M6'-M6) has the same magnitude and phase of the signal of M4 (the same for M4'-M7'-M7 with M5) thus

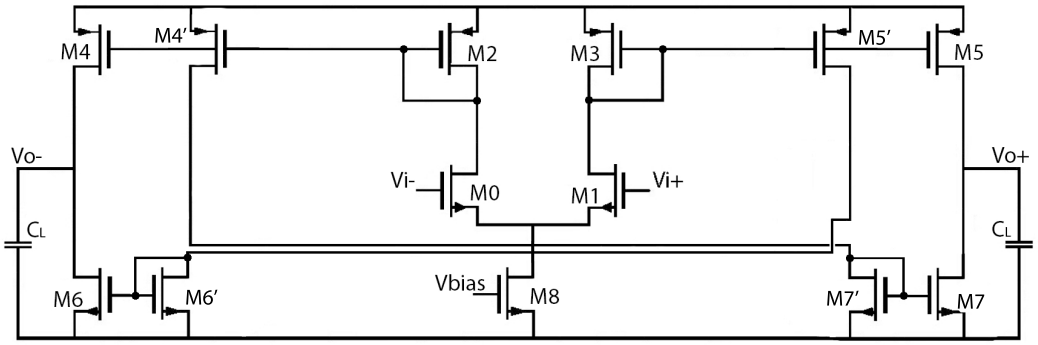

Figure 5.26. Modified Current Mirror Based opamp.

at the output the signal is matematically doubled.The voltage gain of the modified structure is given by:

$$Gain = 2 \cdot gm \cdot K_{Mirror} \cdot R \tag{5.105}$$

wherethe factor 2 comes from the doubled signal's path. This result is very important because allows to obtain the desired matching between the open loop gains of the opamps, avoiding the problems described previously. Indeed, using this approach to obtain the desired factor between the gains of the opamps, both the transconductance, the mirroring factor, and the resistive load are identical in the two opamps.

The opamp that requires less gain is practically identical as shown in figure 5.27, but the signal of the auxiliary branch is deleted, thus the gain:

$$Gain = gm \cdot K \cdot R \tag{5.106}$$

without the factor 2.

5.3.3 Obtain the +2 in the Gain Ratio

The basic principle to get the +2 in the desired ratio $A = 2B + 2$ between the gain of the involved opamps, is add a parallel path by a transconductor, and put its output directly on the load of the opamp as descrived in figure 5.28.

In this way setting the transconductance to $2/R$, the gain contribution of the additional path is:

$$V_o' = V_i \cdot \frac{2}{R} \cdot R \Rightarrow \frac{V_o'}{V_i} = \frac{2}{R} \cdot R = 2 \tag{5.107}$$

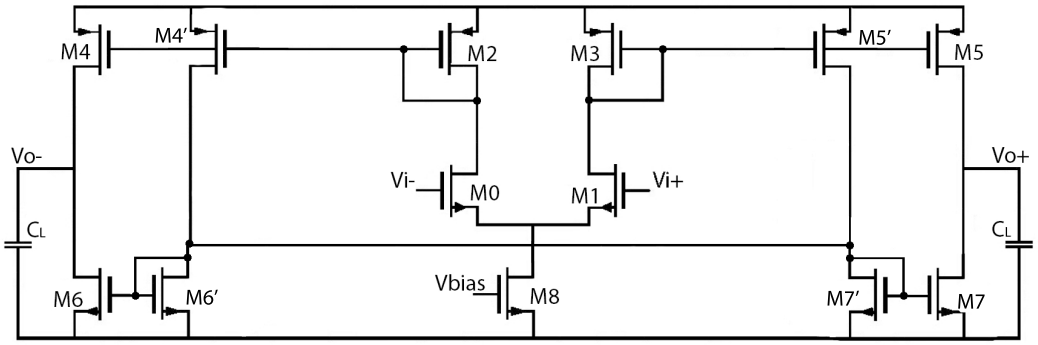

Figure 5.27. CMB opamp with auxiliary branch and gain suppression

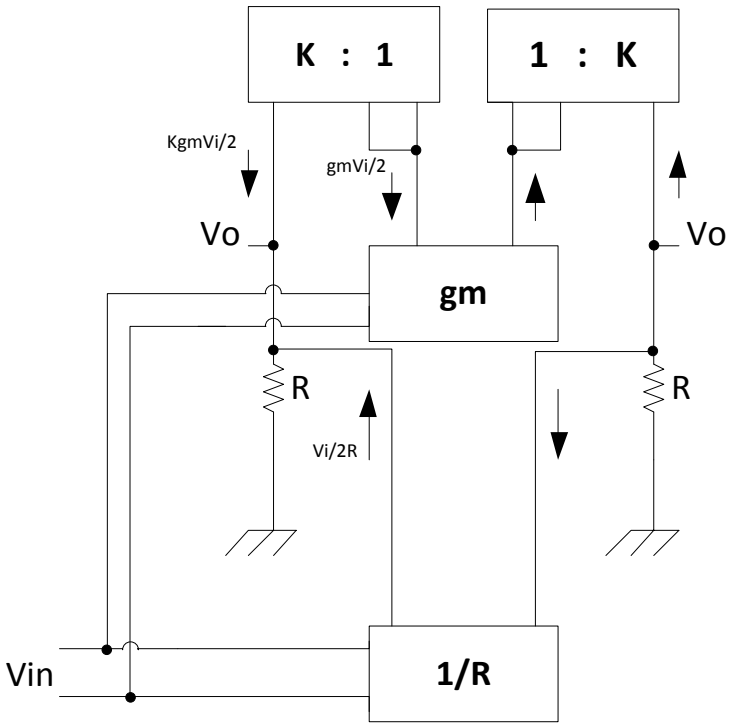

Figure 5.28. Blocks schematic to get gain=A+2

thus the total gain of OPA+OTA is given by:

$$Gain = (gm \cdot K_{mirror} + Gm_{OTA})\, R_{Load} = \left(gm \cdot K_{Mirror} + \frac{1}{R_{OTA}}\right) R_{Load} \tag{5.108}$$

when $R_{OTA} = \frac{1}{2} R_{Load} = R$ the equation 5.108 become:

$$Gain = (gm \cdot K_{Mirror} \cdot R) + 2 \tag{5.109}$$

5.4 Design of an Active-Feedback Based ADC Pipeline

The theory developed at the beginning of this chapter has been used to design the opamps required by the active feedback loop to implement a 100MS/s 12bit pipeline ADC. To achieve the specification of f_u and m_ϕ for each opamp, a two poles transfer function is considered. Imposing a requirement on the settling time, a requirement on the f_{uA} can be obtained:

$$e^{t/\tau} = 2^{-(N+2)} \;\rightarrow\; \frac{t}{\tau} = (N+1)ln(2) \;\rightarrow\; \tau = \frac{T_{Ck}}{2(N+1)ln(2)} \tag{5.110}$$

from which the ω_0 of the system is obtained as $\omega_0 = 1/\tau$, thus $f_0 = \frac{\omega_0}{2\pi}$. Through $\omega_0 = A \cdot p_{1A}$, the frequency of the first pole of the main amplifier can be determined.

$$f_{uA} = \frac{\omega_{uA}}{2\pi} \tag{5.111}$$

Considering 90° the phase contribution of the first pole of the main amplifier at the f_0 (of the whole system), and wanting get $m_{\phi SYS} = 60°$, the total phase contribution of the second pole of the main amplifier and both the poles of the feedback amplifier must be 30° at f_0. Thus considering 5° the phase contribution of the second pole of the main amplifier:

$$arctg\left(\frac{\omega_0}{p_{2A}}\right) = 5 \;\rightarrow\; p_{2A} = \frac{\omega_0}{tan(5)} \tag{5.112}$$

thus, the phase margin of the main opamp is:

$$m_{\phi A} = 90 - arctg\left(\frac{\omega_{uA}}{p_{2A}}\right) \tag{5.113}$$

for the feedback amplifier the total phase contribution introuced is

$$2 \cdot arctan\left(\frac{\omega_0}{\omega_{uB}}\right) = 25 \;\rightarrow\; \omega_{uB} = \frac{\omega_0}{tan(12.5)} \tag{5.114}$$

The design specification for both the amplifiers needed to make the opamp suitable for a 100MS/s pipeline ADC are summarized in table 5.1

Table 5.1. Requirements for the opamps

f_{uA}	250 MHz
$m_{\phi A}$	80 °
f_{uB}	650MHz
$m_{\phi A}$	65 °

Gain	41.01 dB
f_u	788.5 MHz
$m\varphi$	78.3 °
CMRR	276.4 dB
PSRR	261.3 dB
C_{in}	31.78 fF

Table 5.2. Main amplifier characterization

5.4.1 Opamps Characterization

The schematic of the main opamp is already shown in figure 5.26, the feedback amplifier instead is shown in figure 5.29. The feedback amplifier is a Differential Difference Amplifier (DDA), because with a normal fully differential amplifier the non inverting voltage buffer can not be implemented. Thus the x2 between the gains of the involved opamps is due to the different definition of gain in DDA amplifiers.

thus the x2 gain is obtained

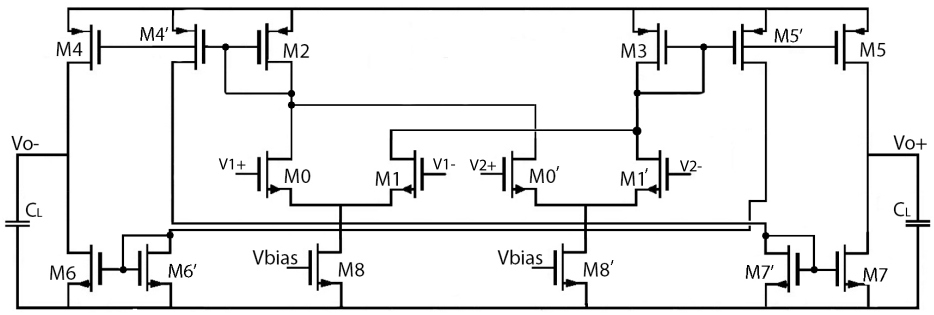

Figure 5.29. Feedback amplifier in DDA version

The opamps, the active feedback chain and the whole ADC pipeline are simulated in STmictoelectronics CMOS 40nm process, the voltage supply is 1.2V, and the value of the capacitive load as the sampling capacitance is 200fF. In the tables 5.2 and 5.3 are reported the characterization in typical process corner and T=27°C for the main and feedback amplifiers.

In tables 5.4 and 5.5 are reported the characterization results of both the

Gain	36.37 dB
f_u	2.01 GHz
$m\varphi$	68.1 °
CMRR	286.57 dB
PSRR	270.67 dB
C_{in}	10.73 fF

Table 5.3. Feedback amplifier characterization

Temp [°C]	0	27	100
Gain [dB]	41.47	41.01	39.91
f_u $[MHz]$	897	817.5	689.9
$m\varphi$ [°]	77.9	78.3	78.79

Table 5.4. Main opamp characterization with temperature variation

amplifiers with temperature variation, and also in tables 5.6 and 5.7 are reported the characterization results for the four process corners.

5.4.2 Active Feedback Characterization

The characterization of the active feedback loop starts from a continuous time implementation. In figure 5.30 the ac-analysis on the open loop structure reveals a dominant pole behaviour, with a f_u of about 550MHz and a phase margin 5° below the desired value. However this reduced value of phase margin does not involve instability, but at the most some effects on the transient response.

From the transient analysis the settling time required for 12 bit accuracy, thus an error below $\epsilon \leq 2^{-(N+1)}$ (with N=12) resuls 14.04ns. Also from the transient analysis result a maximum slew rate of $680mV/nS$ (on a load capacitor of 200fF).

From a DC analysis a linear output dynamic of 700 mV is achieved, this defines the maximum amplitude of the signal allowed to overcome distortion.

In figure 5.31 the closed loop small signal analysis is reported.

Ideally the gain of the MDAC stage will be 2 as long as the capacitors has the

Temp [°C]	0	27	100
Gain [dB]	36.84	36.37	35.284
f_u $[GHz]$	2.2	2.01	1.2
$m\varphi$ [°]	64.3	68.1	93.43

Table 5.5. Feedback opamp characterization with temperature variation

Corner	TYP	SS	SF	FS	FF
Gain [dB]	41.01	40.42	40.69	41.14	41.38
f_u $[MHz]$	817	727.3	775.3	846.2	887.5
$m\varphi$ [°]	78.3	78.39	79	77.77	77.91

Table 5.6. Main opamp characterization with process variation

Corner	TYP	SS	SF	FS	FF
Gain [dB]	36.37	35.77	36.04	36.51	36.74
f_u $[GHz]$	2.01	1.49	1.71	2.06	2.169
$m\varphi$ [°]	67.1	87.52	79.9	66.73	64.43

Table 5.7. Feedback opamp characterization with process variation

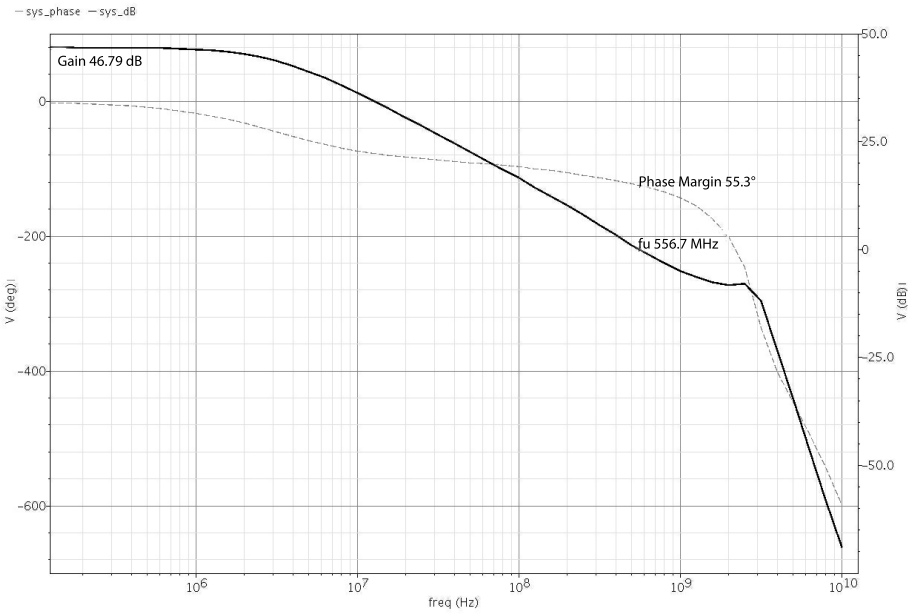

Figure 5.30. ac-analysis of a continuous-time implementation of the active feedback loop

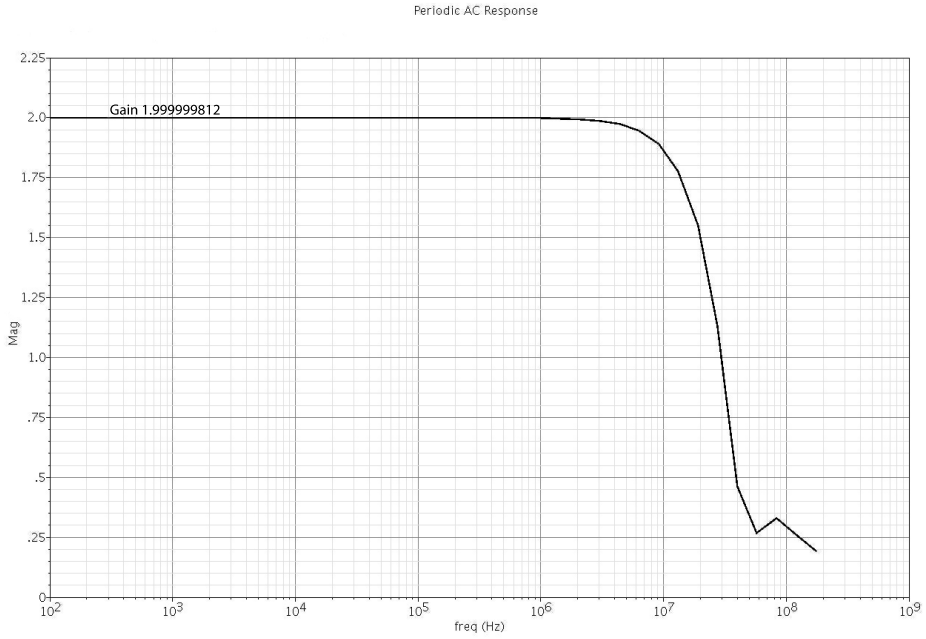

Figure 5.31. Effective closed loop gain

same values. But in actual implementation some capacitive partition due to parasitic capacitance does not allow to reach the desired value. In fact thus from the small signal analysis results a gain of 1.999999812, thus the residue gain error can be determined as $Gain_{ideal} - Gain_{actual} \rightarrow \epsilon_{res} = 188n$. From this value of residue gain error through (5.17) the equivalent gain of a classical feedback structure can be computed as:

$$A_{eq} = \frac{4}{\epsilon_{res}} - 2 \tag{5.115}$$

in this case, with $\epsilon_{res} = 188n$ the equivalent gain reached is 146.55dB.

A Monte Carlo analysis has been performed to confirm the results of the typical case. As shown in figure 5.32 the mean value of the distribution is $\epsilon_{mean} = 934\mu$, this value corresponds to an equivalent gain of 72.6dB, but if the value at the standard deviation is considered, an equivalent gain of 55dB is achieved.

5.4.3 Active Feedback Pipeline ADC Characterization

The active feedback based MDAC was used as building block to implement a 100MS/s 13 bit pipeline ADC. The pipeline take as input a sinusoudal signal of frequency 100/64 MHz and 1.2V peak-to-peak amplitude, and the output is recostructed by an ideal DAC to evaluate the ENOB of the converted signal. In figure 5.33 are reported the input and output signal's waveform for the first ADC of the chain.

The DFT analysis of the recostructed output show a HD3 of 83.2dB and a THD

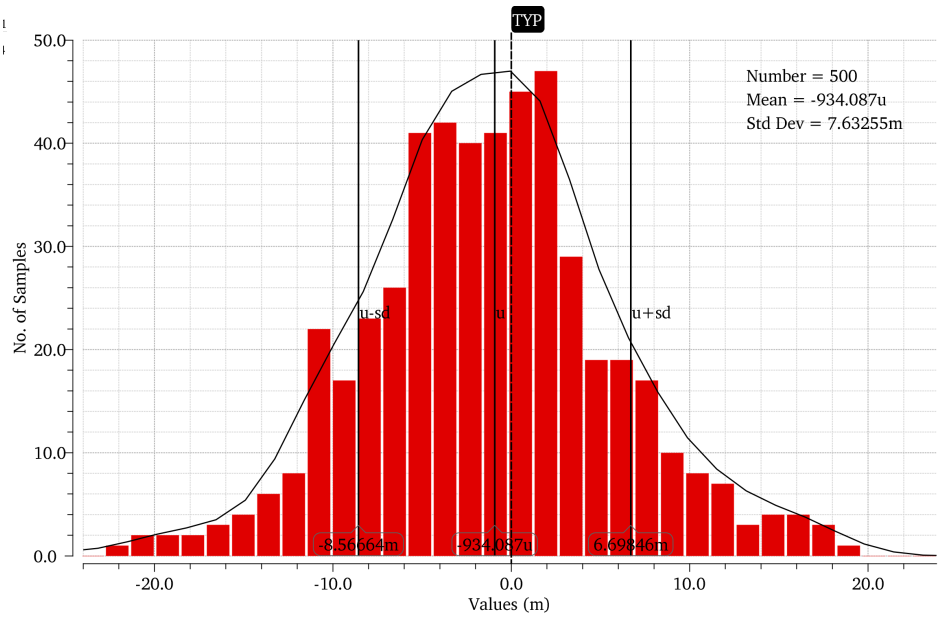

Figure 5.32. Gain error distribution with process variations

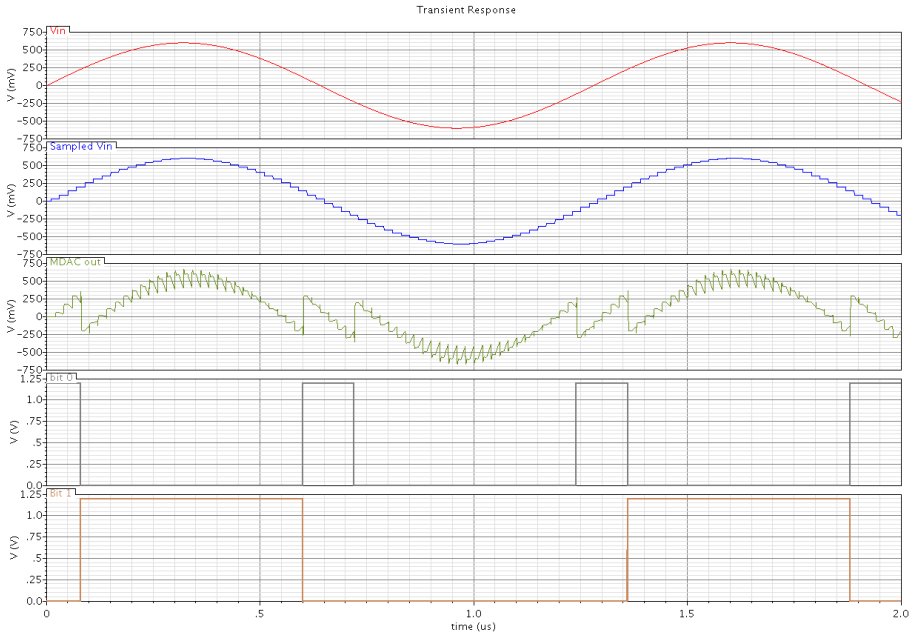

Figure 5.33. Risultato transiente MDAC

of 77.23dB that corresponds to an ENOB of 12.59 bit. Considering the total power dissipated by the ADC of about 38mW, the FOM achieved is 91 fJ/conv. This result shows the effective capability of the active feedback loop to reduce the gain error and consequently increase the linearity of the converter. Furthermore, the resulting FOM says that this technique can be considered suitable to reduce the power consumption of the ADC. In fact for a given accuray of the ADC, the opamps' gain constraints can be relaxed, and then a lower total power consumption is required for single stage, allowing an increase of the FOM of the ADC.

Conclusions

Power consumption plays a fundamental role in electronic devices since realizing low-power circuits allows the increase of battery's life in mobile devices, and both the reduction of the battery size and the heat sink. The reduction of power consumption is always desirable but in some cases it is also mandatory for the feasibility of a system. For example, the feasibility of remote sensing devices, powered by energy harvesting system, is decreed by its energy efficiency.

Digital devices represent most of the semiconductor market, and thus the technology processes are optimized to increase the performance of digital circuits by scaling the size of the devices to increase the integration level on silicon die. Unfortunally the same cannot be said for analog devices, in fact only the transition frequency f_t increases with technology scaling, but other important parameters such as transconductance g_m, output resistance r_0, noise, matching between the devices and signal swing are degraded.

The current approach in integrated circuits market is to integrate both analog and digital circuits on the same die, anyway, many fundamental building blocks, that realize the interface between the analog and digital world can not be considered neither analog nor digital. These interface circuits are called mixed-signal integrated circuits (MS-IC), and in MS-IC design different problem as the intereferences to the analog side are generated by the switching activities of the digital circuit. The MS-ICs are highly attractive for the electronics market because they have the potential of reducing space occupation and power consumption, by substituting many discrete devices, eliminating inter-chip board connections, and increasing hardware reliability.

This thesis has focused the attention on a very useful mixed-signal circuit: the pipeline ADC. The pipeline ADCs are widely used for their energy efficiency in high-precision applications where a resolution of about 10-16 bits and sampling rates above hundreds of Mega-samples per second (telecommunication, radar, etc.) are needed. In the following, three possible way of reducing the power consumption optimization of these data converters have been threated.

In the first one, considering that the large amount of digital processing power, at essentially low energy cost, enables the implementation of techniques which relax the specifications of analog circuits by compensating analog imperfections with digital algorithms. This idea leads to digitally assisted analog circuits, and one of the

most important techniques in this field is digital calibration of analog-to-digital converters. In this context, a calibration technique based on Volterra kernels has been detailed. Specifically, it allows to delete non-linear distortion and memory effect. Experimental results prove the effectiveness of the approach.

In the second one is given a different point of view. In particular, the power consumption of a reconfigurable ADC has been optimized through a dynamic voltage scaling linked to the required conversion frequency. The latter needs that the analog circuits in the converter are able to work with different voltage supply. To this purpose, a voltage-scalable inverter-based opamp has been developed and used as building block to realize a reconfigurable ADC pipeline.

Finally, an analog solution that exploits a novel feedback paradigm to avoid gain error in opamps has been proposed. This technique allows the use of two opamps with relaxed specification instead of a single opamp with stringent requirements. Since achieving an high-gain and a large bandwiths requirement in a single opamp need for high power consumption, we propose an active feedback able to satisfies the same requirements using opamp with very relaxed gain constraints.

All of the proposed apporaches are different ways to reduce the power consumption in ADC pipeline, but that can be easly extended to other ADC structures.

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